

MAX3275 U/D I/O Model

SPICE I/O Macromodels aid in understanding signal integrity issues in electronic systems. Most of Maxim's High Frequency/Fiber Communication ICs utilize input and output (I/O) circuits with Current Mode Logic (CML), Positive Emitter Coupled Logic (PECL), and Low Voltage Differential Signal (LVDS) formats to transfer data into and out of an IC. These models are based on simplified circuit expressions that may include replacement of active circuit elements with ideal controlled voltage and current sources. As such, simulation with macromodels should be treated as 'typical' performance and not relied upon as final proof-of-design. Use of macromodel descriptions is not a substitute for worst-case design analysis, nor for testing real circuits over temperature, supply, and other operating limits.

The output format is provided as ASCII text netlists suitable for generic SPICE. This format is compatible with most versions of SPICE such as PSPICE and HSPICE. Additional information is found in HFAN 6.1 *Input/Output Models for Maxim Fiber Components*.

To extract the circuit netlists using the Adobe Acrobat Reader follow these instructions. Select the "Text Select Tool" by clicking the left mouse button on this icon of the menu bar (a capital T with a small dashed box to the lower right). Highlight the desired netlist text with the cursor. Use the copy command from the edit menu to capture the selected lines. Then paste the selected lines into a text file editor and save the file with an extension compatible with the simulator.

Version A, August 15, 2003

MAX3275 Transimpedance Amplifier

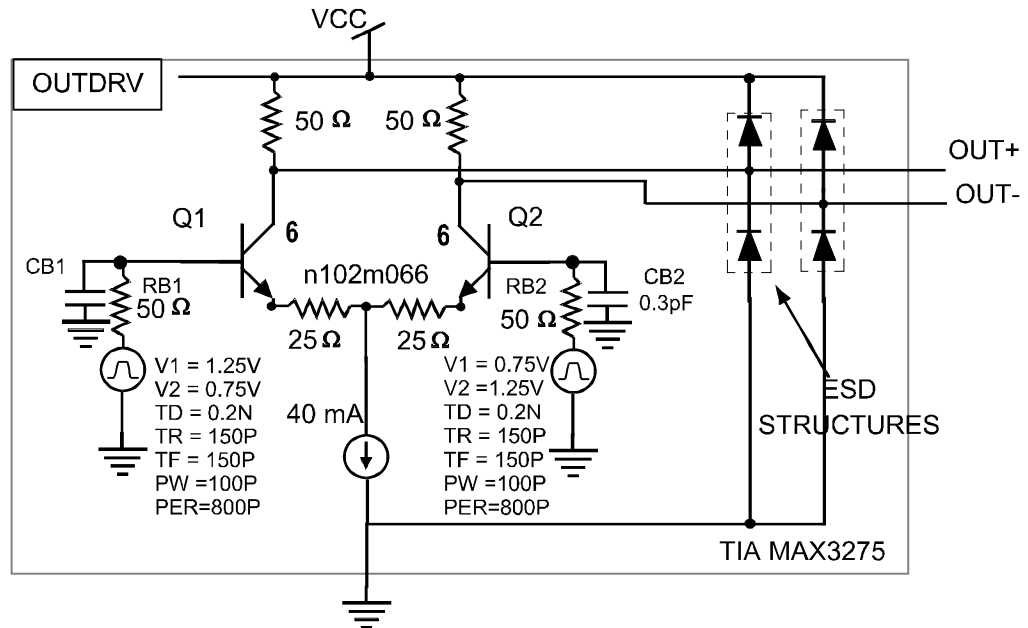


Figure 1. Output signal buffer for the MAX3275 used in dice form. For bondwires estimate 0.9nH/mm and 0.04Ohms/mm.

Notes:

The schematic on the previous page represents the input stage of the Maxim MAX3275C/D Transimpedance amplifiers. The input stage is not modeled since the electrical model is not considered an adequate representation for the analysis of the input optical signal.

The netlist is in SPICE 2g6 format. Since nodes in SPICE 2g6 can only be numbers, the output signals are 2101 and 2102 and the input signals to the die are 1001 and 1002. Comments in the netlist identify the correspondence between the signal names and the node numbers. The netlists are in SPICE 2g6 format and are compatible with PSPICE and HSPICE. It has been simulated on a generic SPICE simulator and PSPICE.

The Output Stage: The input stage is comprised of one subcircuit DRV_OUT. RB1, RB2, CB1 and CB2 can be adjusted to slow or speed up the output signals

Text File Format: This model is shipped in “pdf” format. Models and netlists can be copied to text format in the Acrobat Reader by holding the left mouse button on the “Text Select Tool.” Then the user can “select” what netlist and/or subcircuit with the mouse. Then use the copy command from the “edit” menu to capture the selected lines. These lines can then be “pasted” into the user’s text file.

Circuit Netlist – Output Circuit

```
INPUT - MAX3275U/D OUTPUT CIRCUIT
*
*
.OPTIONS ACCT NOMOD NOPAGE LIMPTS=10000 RELTOL=.001
.WIDTH OUT=80
.TEMP 26
* TYPICAL DIE TEMP = 25C + 0.143W*(6.7C/W) = 26C
.OP
.TRAN 5PS 1500PS
*
* CONVENTIONS VCC = 101, VEE = 102, + OUT = 2000, - OUT = 2002
*
VCC 101 0 DC 3.3
RTERM1 2001 101 100
RTERM2 2002 101 100
RLOAD1 2001 2002 100
CLOAD1 2001 101 0.20P
CLOAD2 2002 101 0.20P
CLOAD3 2001 2002 0.05P

*XPK1 2001 2002 2010 2011 0 0 0 OUTPKG
XCIROUT 2001 2002 101 OUTDRV
*
.SUBCKT OUTDRV 71 72 101
VINP 2 0 PULSE (1.25 0.95 0.2N 0.100N 0.100N 0.30N 0.800N)
VINN 3 0 PULSE (0.95 1.25 0.2N 0.100N 0.100N 0.30N 0.800N)
*
RB1 2 22 50
CB1 22 0 .01p
* Adjusted to match waveform of data sheet
RB2 3 32 50
CB2 32 0 .01p
* Adjusted to match waveform of data sheet
*
XQ1 71 22 64 0 N102M066

XQ3 72 32 65 0 N102M066

RE1 64 63 25
RE2 65 63 25
*

RC1 71 101 50
RC2 72 101 50

*
IE1 63 0 40M
CE1 63 0 .015p

XPAD1 71 0 PAD4OCT3
XESD1 71 101 0 DE0396
XESD2 0 71 0 DE0396
XPAD2 72 0 PAD4OCT3
XESD3 71 101 0 DE0396
XESD4 0 71 0 DE0396

.ENDS OUTDRV
*
```

```

*
*
*
** BEGINNING OF PROCESS LIB
*
.SUBCKT N102M066 1 2 3 21
*scale of 6
CP1SUB 2 201 9.385F
RP1SUB 20 201 100K
CTRENCH 1 202 47.287F
RFIELDDEPI 202 21 202.922
RREVERT 202 20 1G
CBL 10 20 11.869F
RSUB 20 21 56.435K
CWAFAER 20 21 9.335F
CP1EPI 10 12 11.504F
CP1P2 12 3 13.268F
RBX 2 12 11.979 TC=1.934M
RCX 1 10 3.386 TC=2.640M,410.600N
RCI 10 11 846.613M TC=2.640M,410.600N
REX 13 3 2.117
QN 11 12 13 11 TX 6
*XREPORT1 0 REPORTERL1N11
*XREPORT2 0 REPORTERL1N12
.MODEL TX NPN( IS=6.926E-018 XTI=3 EG=1.120 BF=380 BR=12 XTB=0 VAF=66
+ VAR=2.500 NF=1.018 NR=1.020 NE=2 NC=1.560 IKF=15.238M IKR=432.900U
+ ISE=3.463E-018 ISC=1.558E-030 RB=17.968 RBM=13.476 IRB=1.558M
+ CJE=16.207F MJE=463M VJE=1.100 FC=990M CJC=7.862F MJC=350M VJC=1
+ TF=1.320P TR=5N XTF=2 VTF=1.200 ITF=56.277M PTF=5 KF=23.354N
+ AF=2.150 )
.ENDS N102M066

.SUBCKT PAD4OCT3 1 3
CPAD 1 10 41.303F
REPI 10 20 526.050 TC=4.800M,5U
CTRENCH 21 20 19.684F
CBL 21 20 1.079P
RX 20 21 1G
RS 3 21 6.858K
CWAFAER 21 3 1.975F
*XREPORT1 0 REPORTERL1N36
.ENDS PAD4OCT3

.SUBCKT DE0396 1 2 21
CTRENCH 2 202 33.018F
RFIELDDEPI 202 21 291.149
RREVERT 202 21 1G
CBL 4 5 37.842F
RSUB 5 21 49.887K
CWAFAER 5 21 10.560F
CP1EPI 1 4 32.900F
DD 1 4 DCB
RS 4 2 12.010 TC=4.306M,4.262U
*XREPORT1 0 REPORTERL1N27
*XREPORT2 0 REPORTERL1N28
.MODEL DCB D( IS=3.485E-018 N=1.050 CJO=95.040F VJ=800M M=500M )
.ENDS DE0396

.SUBCKT OUTPKG 101 102 201 202 401 402 403
*

```

```
* resistors
*
RB01 201 301 0.25
RB02 202 302 0.25
*
* inductors
*
LLAP_1_3 101 301 1.2N
LLAP_2_4 102 302 1.3N
K02_03 LLAP_1_3 LLAP_2_4 0.294

*LB03 PADT PADBOT 23P
*
* capacitors
*
C01 101 403 143F
C02 102 403 143F
*
* mutual capacitors
*
C01_02 101 102 43.800F
.ENDS OUTPKG
*
.PRINT TRAN V(2001) V(2002)
*.PROBE
*
.END
```