

MAX3265 I/O Model

SPICE I/O Macromodels aid in understanding signal integrity issues in electronic systems. Most of Maxim's High Frequency/Fiber Communication ICs utilize input and output (I/O) circuits with Current Mode Logic (CML), Positive Emitter Coupled Logic (PECL), and Low Voltage Differential Signal (LVDS) formats to transfer data into and out of an IC. These models are based on simplified circuit expressions that may include replacement of active circuit elements with ideal controlled voltage and current sources. As such, simulation with macromodels should be treated as 'typical' performance and not relied upon as final proof-of-design. Use of macromodel descriptions is not a substitute for worst-case design analysis, nor for testing real circuits over temperature, supply, and other operating limits.

The output format is provided as ASCII text netlists suitable for generic SPICE. This format is compatible with most versions of SPICE such as PSPICE and HSPICE. Additional information is found in HFAN 6.1 *Input/Output Models for Maxim Fiber Components*.

To extract the circuit netlists using the Adobe Acrobat Reader follow these instructions. Select the "Text Select Tool" by clicking the left mouse button on this icon of the menu bar (a capital T with a small dashed box to the lower right). Highlight the desired netlist text with the cursor. Use the copy command from the edit menu to capture the selected lines. Then paste the selected lines into a text file editor and save the file with an extension compatible with the simulator.

Version A, March 24 2003

MAX3265 1.25/2.5Gbps Limiting Amplifier

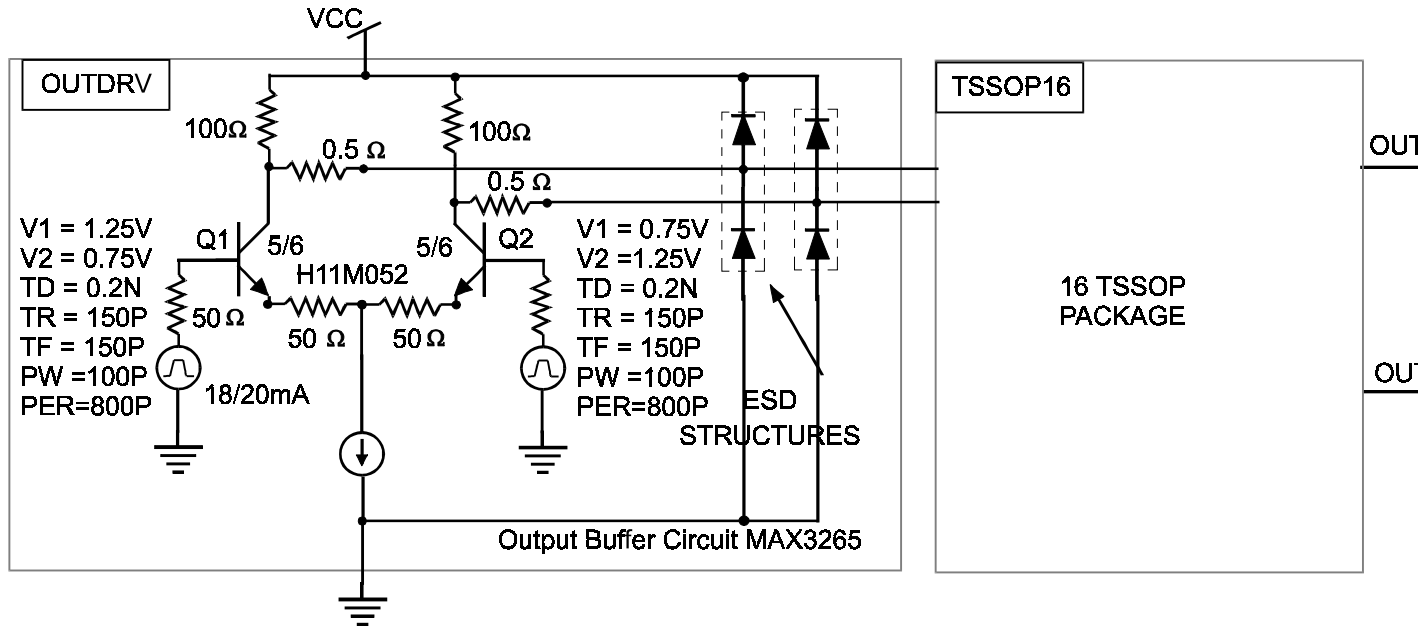


Figure 1. Output signal buffer for the MAX3265 including a simplified package model.

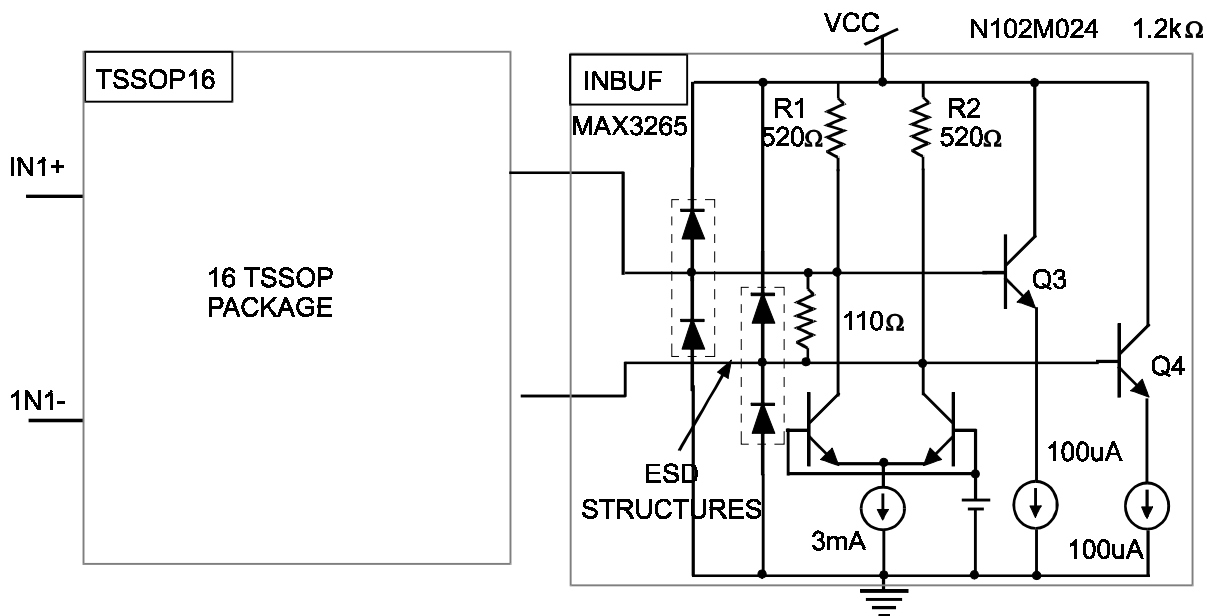


Figure 2. Simplified input package model and input circuitry for the MAX3265.

Notes:

MAX3265 Input Model

The input structure of the MAX3265 is connected to a differential common-emitter amplifier that is designed to compensate for internal device mismatches. In the actual circuit there is a feedback path that controls the differential amplifier to adjust the input biasing points and compensate for any device mismatch. This model does not attempt to model the offset correction functionality, but the amplifier is included to account for any parasitic impedance that it presents to the input pins.

The input pins are nodes 101 (IN+) and 102 (IN-). These are connected to a model pattern generator that includes 50Ω output impedance and AC coupling. The pattern generator has two $1M\Omega$ resistors connected to ground to provide a DC path to ground at these nodes, which is a requirement of the Spice simulator.

The driving voltage source (VIN) should be set to 0V differential at $t=0$. This ensures that the two AC coupling capacitors are not charged to different voltages initially. (This is the way the circuit operates in steady-state operation.) I achieved this condition by using a piecewise linear source as my driver, with a voltage of 0V at $t=0$. The swing applied to the input can be varied across the acceptable range of input for the MAX3265, which is $10mV_{P-P}$ to $1200mV_{P-P}$. Remember that there is a 50% drop across the 50Ω output impedance of the generator, so to get a $10mV_{P-P}$ swing at the input the MAX3265 the source should swing between +10mV and -10mV (a $20mV_{P-P}$ swing).

MAX3265 CML Output Model

The CML output model is a simplified version of the output stage used by the MAX3265 limiting amplifier. The package model is quite accurate, and the output impedance presented by the output emitter-followers should also be fairly accurate. Simplifications have been made regarding performance over temperature, so the model is only accurate at a temperature of $35^{\circ}C$. Operation at other temperatures will give very different results than the actual MAX3265 output. The model was not compensated for variation in VCC, so $VCC=3.3V$ should be used.

The output current of the MAX3265 can be set to two levels, either 18 mA or 20mA. The control signal "LEVEL" is not modeled, however the current may be lowered to 18mA in the netlist by setting the current source IB2 to .01mA. The netlist includes the external resistors to set the termination to 50 Ohms. A load resistance of 100 Ohms is also included. The output pins are nodes 2001 (OUT-) and 2002 (OUT+).

Text File Format: This model is shipped in “pdf” format. Models and netlists can be copied to text format in the Acrobat Reader by holding the left mouse button on the “Text Select Tool.” Then the user can “select” what netlist and/or subcircuit with the mouse. Then use the copy command from the “edit” menu to capture the selected lines. These lines can then be “pasted” into the user’s text file. Make sure to save the text file as plain text without any formatting.

Circuit Netlist – Input circuit

```
INPUT - MAX3265 INPUT CIRCUIT
*
* THIS IS THE TYPICAL INPUT OF THE MAX3265
* IN+ IS NODE 101 AND IN- IS NODE 102
*

.OPTIONS ACCT NOMOD NOPAGE LIMPTS=1000000 RELTOL=.001

.WIDTH OUT=80

.TEMP 35

.OP
.TRAN 2P 1.7N

* DRIVER *****
VIN 81 82 PWL(0 0 50P 600M 350P 600M 450P -600M 750P -600M 850P 600M)
R6 81 91 50
R5 82 92 50
C1 91 101 0.1U
C2 92 102 0.1U
R21 81 0 1MEG
R22 82 0 1MEG
*****

VCC 1 0 DC 3.3

XESD1P 1001 1 0 HDE113032
XESD1M 0 1001 0 HDE113032
XESD2P 1002 1 0 HDE113032
XESD2M 0 1002 0 HDE113032

XR1 1001 1 0 HRND520
XR2 1002 1 0 HRND520
XR3 1001 1002 0 HRND110

XPK1 0 0 0 101 102 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1001 1002 0 0 0 0
+
0 0 0 0 0 0 0 0 0 0 TSSOP16
XQ1a 1001 3 4 0 H11M05
XQ1b 1001 3 4 0 H11M05
XQ1c 1001 3 4 0 H11M05

XQ2a 1002 3 4 0 H11M05
XQ2b 1002 3 4 0 H11M05
XQ2c 1002 3 4 0 H11M05

XQ3a 1 1001 2001 0 H12A05
XQ3b 1 1001 2001 0 H12A05

XQ4a 1 1002 2002 0 H12A05
XQ4b 1 1002 2002 0 H12A05

I1 4 0 3M
I2 2002 0 1M
I3 2001 0 1M
VOFFSET 3 0 2

*****
.SUBCKT H12A05 1 2 3 21
CP1EPI 1 2 7.147F
```

```

CP1P2 12 3 12.915F
CTRENCH 1 20 10.524F
RBX 2 12 30.538 TC=2.649M
RCX 1 10 35.869 TC=2.315M,931.161N
RCI 10 11 1.888 TC=2.315M,931.161N
REX 13 3 4.328 TC=182.441U
RSUB 20 21 9.008K
QP 20 10 12 20 TXP OFF
QN 11 12 13 11 TX
.MODEL TX NPN( IS=2.302E-017 XTI=3 EG=1.140 BF=223.719 BR=20 XTB=450M
+ VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=88.032M
+ IKR=1.613M ISE=1.089E-020 ISC=1.400E-029 RB=30.538 RBM=22.904
+ IRB=14M CJE=74.302F MJE=490M VJE=940M FC=990M CJC=14.718F MJC=470M
+ VJC=850M TF=3.814P TR=19N XTF=1 VTF=1K ITF=40.860M PTF=5 KF=1.500F
+ AF=1 )
.MODEL TXP PNP( IS=1.308E-018 CJE=14.718F MJE=470M VJE=850M CJC=13.849F
+ MJC=400M VJC=650M BF=10K BR=869.864U TF=1N FC=900M )
.ENDS H12A05
*****

*****
.SUBCKT H11M05 1 2 3 21
CP1EPI 1 2 2.192F
CP1P2 12 3 6.473F
CTRENCH 1 20 7.654F
RBX 2 12 164.841 TC=1.611M
RCX 1 10 40.687 TC=2.961M,1.642U
RCI 10 11 2.141 TC=2.961M,1.642U
REX 13 3 7.711 TC=57.819U
RSUB 20 21 14.233K
QP 20 10 12 20 TXP OFF
QN 11 12 13 11 TX
.MODEL TX NPN( IS=1.151E-017 XTI=3 EG=1.140 BF=223.719 BR=20 XTB=450M
+ VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=44.016M
+ IKR=806.400U ISE=5.444E-021 ISC=7.000E-030 RB=164.841 RBM=123.631
+ IRB=7M CJE=37.151F MJE=490M VJE=940M FC=990M CJC=7.359F MJC=470M
+ VJC=850M TF=3.814P TR=19N XTF=1 VTF=1K ITF=20.430M PTF=5 KF=1.500F
+ AF=1 )
.MODEL TXP PNP( IS=6.540E-019 CJE=7.359F MJE=470M VJE=850M CJC=7.985F
+ MJC=400M VJC=650M BF=10K BR=924.230U TF=1N FC=900M )
.ENDS H11M05
*****

*****
* TSPICE CONVERSION TO SPICE2G.6
*created Fri May 10 14:56:27 2002
*
*
.SUBCKT HDE113032 1 2 21
CP1EPI 1 4 88.881F
QD 5 4 1 5 QESD
RS 4 2 2.531 TC=2.729M,1.896U
RSUB 5 21 2.936K
CTRENCH 2 5 22.961F
.MODEL QESD PNP( IS=1.181E-017 NF=1.050 BF=800M BR=600U CJE=155.018F
+ VJE=600M MJE=400M CJC=53.258F VJC=650M MJC=400M )
.ENDS HDE113032
*****

*****
* TSPICE CONVERSION TO SPICE2G.6
*created Tue Jul 02 11:07:54 2002
*
*
.SUBCKT HRND520 1 2 3
R1 1 4 260 TC=150U

```

R2 4 2 260 TC=150U
C1 1 3 82.558F
C2 4 3 165.116F
C3 2 3 82.558F
.ENDS HRND520

* TSPICE CONVERSION TO SPICE2G.6
*created Tue Jul 02 09:55:20 2002
*
*

.SUBCKT HRND110 1 2 3
R1 1 4 55 TC=150U
R2 4 2 55 TC=150U
C1 1 3 52.896F
C2 4 3 105.793F
C3 2 3 52.896F
.ENDS HRND110

* TSPICE CONVERSION TO SPICE2G.6
*created Wed Jun 26 10:34:04 2002

* Pad->Lead Frame side 2 Lead Pin 1 Chip side 17
* Pad->Lead Frame side 3 Lead Pin 2 Chip side 18
* Pad->Lead Frame side 4 Lead Pin 3 Chip side 19
* Pad->Lead Frame side 5 Lead Pin 4 Chip side 20
* Pad->Lead Frame side 6 Lead Pin 5 Chip side 21
* Pad->Lead Frame side 7 Lead Pin 6 Chip side 22
* Pad->Lead Frame side 8 Lead Pin 7 Chip side 23
* Pad->Lead Frame side 9 Lead Pin 8 Chip side 24
* Pad->Lead Frame side 10 Lead Pin 9 Chip side 25
* Pad->Lead Frame side 11 Lead Pin 10 Chip side 26
* Pad->Lead Frame side 12 Lead Pin 11 Chip side 27
* Pad->Lead Frame side 13 Lead Pin 12 Chip side 28
* Pad->Lead Frame side 14 Lead Pin 13 Chip side 29
* Pad->Lead Frame side 15 Lead Pin 14 Chip side 30
* Pad->Lead Frame side 16 Lead Pin 15 Chip side 31
* Pad->Padtop = 32
* Pad->Padbot = 33
* Pad->GND = 34

.SUBCKT TSSOP16 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
+ 24 25 26 27 28 29 30 31 32 33 34

*
* resistors
*

RB01 17 35 59M
RB02 18 36 65M
RB03 19 37 66M
RB04 20 38 61M
RB05 21 39 59M
RB06 22 40 65M
RB07 23 41 65M
RB08 24 42 58M
RB09 25 43 59M
RB10 26 44 65M
RB11 27 45 65M
RB12 28 46 59M
RB13 29 47 61M
RB14 30 48 66M
RB15 31 49 65M

*

* inductors

*

LLAP_1_16 2 35 2.59e-009
LLAP_2_17 3 36 2.27e-009
LLAP_3_18 4 37 1.9e-009
LLAP_4_19 5 38 1.79e-009
LLAP_5_20 6 39 1.74e-009
LLAP_6_21 7 40 1.87e-009
LLAP_7_22 8 41 2.26e-009
LLAP_8_23 9 42 2.62e-009
LLAP_9_24 10 43 2.6e-009
LLAP_10_25 11 44 2.29e-009
LLAP_11_26 12 45 1.9e-009
LLAP_12_27 13 46 1.76e-009
LLAP_13_28 14 47 1.79e-009
LLAP_14_29 15 48 1.91e-009
LLAP_15_30 16 49 2.28e-009
KL_1_2 LLAP_1_16 LLAP_2_17 0.3122
KL_1_3 LLAP_1_16 LLAP_3_18 0.113148
KL_1_4 LLAP_1_16 LLAP_4_19 0.0626985
KL_2_3 LLAP_2_17 LLAP_3_18 0.207052
KL_2_4 LLAP_2_17 LLAP_4_19 0.10021
KL_2_5 LLAP_2_17 LLAP_5_20 0.0508199
KL_3_4 LLAP_3_18 LLAP_4_19 0.254314
KL_3_5 LLAP_3_18 LLAP_5_20 0.122646
KL_3_6 LLAP_3_18 LLAP_6_21 0.0594183
KL_4_5 LLAP_4_19 LLAP_5_20 0.25725
KL_4_6 LLAP_4_19 LLAP_6_21 0.115328
KL_5_6 LLAP_5_20 LLAP_6_21 0.247252
KL_5_7 LLAP_5_20 LLAP_7_22 0.0963173
KL_5_8 LLAP_5_20 LLAP_8_23 0.0557342
KL_6_7 LLAP_6_21 LLAP_7_22 0.213059
KL_6_8 LLAP_6_21 LLAP_8_23 0.110235
KL_7_8 LLAP_7_22 LLAP_8_23 0.304107
KL_9_10 LLAP_9_24 LLAP_10_25 0.309416
KL_9_11 LLAP_9_24 LLAP_11_26 0.11293
KL_9_12 LLAP_9_24 LLAP_12_27 0.0649788
KL_10_11 LLAP_10_25 LLAP_11_26 0.21861
KL_10_12 LLAP_10_25 LLAP_12_27 0.113569
KL_11_12 LLAP_11_26 LLAP_12_27 0.264128
KL_11_13 LLAP_11_26 LLAP_13_28 0.113329
KL_11_14 LLAP_11_26 LLAP_14_29 0.0587929
KL_12_13 LLAP_12_27 LLAP_13_28 0.247333
KL_12_14 LLAP_12_27 LLAP_14_29 0.1189
KL_13_14 LLAP_13_28 LLAP_14_29 0.262841
KL_13_15 LLAP_13_28 LLAP_15_30 0.10791
KL_14_15 LLAP_14_29 LLAP_15_30 0.212285

*LB16 32 33 25P

*

* capacitors

*

C01 2 34 235F
C02 3 34 194F
C03 4 34 181F
C04 5 34 181F
C05 6 34 181F
C06 7 34 181F
C07 8 34 194F
C08 9 34 235F
C09 10 34 235F
C10 11 34 194F
C11 12 34 182F
C12 13 34 182F
C13 14 34 181F
C14 15 34 181F

```

C15 16 34 194F
*
* mutual capacitors
*
C01_02 2 3 127F
C02_03 3 4 47.800F
C03_04 4 5 44.800F
C04_05 5 6 44F
C05_06 6 7 44.700F
C06_07 7 8 47.800F
C07_08 8 9 127F
C09_10 10 11 127F
C10_11 11 12 47.800F
C11_12 12 13 44.700F
C12_13 13 14 44F
C13_14 14 15 44.800F
C14_15 15 16 47.800F
.ENDS TSSOP16
*****

.PRINT TRAN V(101) V(102)

.END

```

Circuit Netlist – Output circuit

```

INPUT - MAX3265 OUTPUT CIRCUIT
*
* THIS IS THE TYPICAL CML OUTPUT OF THE MAX3265
*
.OPTIONS ACCT NOMOD NOPAGE LIMPTS=10000 RELTOL=.001
.WIDTH OUT=80
.TEMP 35
* TYPICAL DIE TEMP = 25C + 2.2W*(26C/W) = 80C
.OP
.TRAN 5PS 1500PS
*
* CONVENTIONS VCC = 101, VEE = 102, + OUT = 2000, - OUT = 2002
*
VCC 101 0 DC 3.3
RTERM1 2001 101 100
RTERM2 2002 101 100
RLOAD1 2001 2002 100
CLOAD1 2001 101 0.20P
CLOAD2 2002 101 0.20P
CLOAD3 2001 2002 0.05P
XPK1 0 0 0 0 0 0 0 0 0 0 0 101 2001 2002 101 0 0 0 0 0 0 0 0 0 0
+      0 101 1001 1002 101 0 0 0 0 TSSOP16

XCIROUT 1001 1002 101 OUTDRV
*
.SUBCKT OUTDRV 1001 1002 101
VINP 2 0 PULSE (1.25 0.95 0.2N 0.150N 0.150N 0.250N 0.800N)
VINN 3 0 PULSE (0.95 1.25 0.2N 0.150N 0.150N 0.250N 0.800N)
*
RB1 2 22 50
RB2 3 32 50
*
XQ10 71 22 61 0 H11M052
XQ11 71 22 61 0 H11M052
XQ12 71 22 61 0 H11M052
XQ13 71 22 61 0 H11M052
XQ14 71 22 61 0 H11M052

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*
XQ20 72 32 62 0 H11M052
XQ21 72 32 62 0 H11M052
XQ22 72 32 62 0 H11M052
XQ23 72 32 62 0 H11M052
XQ24 72 32 62 0 H11M052

XQ30 71 22 64 0 H11M052
XQ31 71 22 64 0 H11M052
XQ40 72 32 65 0 H11M052
XQ41 72 32 65 0 H11M052
*
RC1 71 101 100
RF1 1001 71 0.5
RC2 72 101 100
RF2 1002 72 0.5
*
IB1 63 0 18M
IB2 66 0 2M
*IB2 66 0 0.01M
RC3 63 62 50
RC4 63 61 50
RC5 66 64 50
RC6 66 65 50
*
*XPAD1 1001 101 0 0 PADESD100
*XPAD2 1002 101 0 0 PADESD100

XPAD1 1001 0 HPAD3
XPAD2 1002 0 HPAD3
XESD1P 1001 1 0 HDE113032
XESD1M 0 1001 0 HDE113032
XESD2P 1002 1 0 HDE113032
XESD2M 0 1002 0 HDE113032
*
.ENDS OUTDRV
*
*
** BEGINNING OF PROCESS LIB
*

.SUBCKT DESD 1 2 21
CP1EPI 1 4 8.743F
QD 5 4 1 5 QESD
*dd 1 4 dcb : area=count
*ds 5 4 dsub : area=count
RS 4 2 32.058 TC=2.813M,2.043U
RSUB 5 21 16.621K
CTRENCH 2 5 6.455F
.MODEL QESD PNP( IS=6.109E-019 NF=1.050 BF=800M BR=600U CJE=12.463F
+ VJE=640M MJE=330M CJC=5.346F VJC=790M MJC=460M )
.ENDS DESD

.SUBCKT PADESD100 2 3 4 5
CXP1 2 5 50F
XQ1 2 3 5 DE381011
XQ2 4 2 5 DE381011
.ENDS PADESD100

.SUBCKT DE381011 1 2 21
CP1EPI 1 4 132.715F
QD 5 4 1 5 QESD
RS 4 2 2.024 TC=2.615M,1.746U
RSUB 5 21 2.318K
CTRENCH 2 5 38.731F

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.MODEL QESD PNP( IS=1.080E-017 NF=1.050 BF=800M BR=600U CJE=220.280F
+ VJE=640M MJE=330M CJC=75.512F VJC=790M MJC=460M )
.ENDS DE381011
*
*
.SUBCKT H11M052 1 2 3 21
CP1EPI 1 2 2.192F
CP1P2 12 3 6.473F
CTRENCH 1 20 7.654F
RBX 2 12 82.961 TC=2.214M
RCX 1 10 40.687 TC=2.961M,1.642U
RCI 10 11 2.141 TC=2.961M,1.642U
REX 13 3 7.711 TC=57.819U
RSUB 20 21 14.233K
QP 20 10 12 20 TXP OFF
QN 11 12 13 11 TX
*XREPORT1 0 REPORTERL1N13
*XREPORT2 0 REPORTERL1N8
.MODEL TX NPN( IS=1.151E-017 XTI=3 EG=1.140 BF=223.719 BR=20 XTB=450M
+ VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=44.016M
+ IKR=806.400U ISE=5.444E-021 ISC=7.000E-030 RB=82.961 RBM=62.221
+ IRB=7M CJE=37.151F MJE=490M VJE=940M FC=990M CJC=7.359F MJC=470M
+ VJC=850M TF=3.814P TR=19N XTF=1 VTF=1K ITF=20.430M PTF=5 KF=1.500F
+ AF=1 )
.MODEL TXP PNP( IS=6.540E-019 CJE=7.359F MJE=470M VJE=850M CJC=7.985F
+ MJC=400M VJC=650M BF=10K BR=924.230U TF=1N FC=900M )
.ENDS H11M052
*
*
.SUBCKT HPAD3 1 3
CPAD 1 10 86.407F
REPI 10 20 149.204M TC=4.800M,5U
CTRENCH 21 20 79.795F
DS 21 20 DSUB
RS 3 21 369.115
*XREPORT1 0 REPORTERL1N94
.MODEL DSUB D( IS=98.719F CJO=555.750F M=400M VJ=650M )
.ENDS HPAD3
*
*
.SUBCKT HDE113032 1 2 21
CP1EPI 1 4 88.881F
QD 5 4 1 5 QESD
RS 4 2 2.531 TC=2.729M,1.896U
RSUB 5 21 2.936K
CTRENCH 2 5 22.961F
.MODEL QESD PNP( IS=1.181E-017 NF=1.050 BF=800M BR=600U CJE=155.018F
+ VJE=600M MJE=400M CJC=53.258F VJC=650M MJC=400M )
.ENDS HDE113032
*
*
* TSPICE CONVERSION TO SPICE2G.6
*created Wed Jun 26 10:34:04 2002

* Pad->Lead Frame side 2 Lead Pin 1 Chip side 17
* Pad->Lead Frame side 3 Lead Pin 2 Chip side 18
* Pad->Lead Frame side 4 Lead Pin 3 Chip side 19
* Pad->Lead Frame side 5 Lead Pin 4 Chip side 20
* Pad->Lead Frame side 6 Lead Pin 5 Chip side 21
* Pad->Lead Frame side 7 Lead Pin 6 Chip side 22
* Pad->Lead Frame side 8 Lead Pin 7 Chip side 23
* Pad->Lead Frame side 9 Lead Pin 8 Chip side 24
* Pad->Lead Frame side 10 Lead Pin 9 Chip side 25
* Pad->Lead Frame side 11 Lead Pin 10 Chip side 26
* Pad->Lead Frame side 12 Lead Pin 11 Chip side 27
* Pad->Lead Frame side 13 Lead Pin 12 Chip side 28
* Pad->Lead Frame side 14 Lead Pin 13 Chip side 29

```

```

* Pad->Lead Frame side 15 Lead Pin 14 Chip side 30
* Pad->Lead Frame side 16 Lead Pin 15 Chip side 31
* Pad->Padtop = 32
* Pad->Padbot = 33
* Pad->GND = 34

*
*
.SUBCKT TSSOP16 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
+ 24 25 26 27 28 29 30 31 32 33 34
*
* resistors
*
RB01 17 35 59M
RB02 18 36 65M
RB03 19 37 66M
RB04 20 38 61M
RB05 21 39 59M
RB06 22 40 65M
RB07 23 41 65M
RB08 24 42 58M
RB09 25 43 59M
RB10 26 44 65M
RB11 27 45 65M
RB12 28 46 59M
RB13 29 47 61M
RB14 30 48 66M
RB15 31 49 65M
*
* inductors
*
LLAP_1_16 2 35 2.59e-009
LLAP_2_17 3 36 2.27e-009
LLAP_3_18 4 37 1.9e-009
LLAP_4_19 5 38 1.79e-009
LLAP_5_20 6 39 1.74e-009
LLAP_6_21 7 40 1.87e-009
LLAP_7_22 8 41 2.26e-009
LLAP_8_23 9 42 2.62e-009
LLAP_9_24 10 43 2.6e-009
LLAP_10_25 11 44 2.29e-009
LLAP_11_26 12 45 1.9e-009
LLAP_12_27 13 46 1.76e-009
LLAP_13_28 14 47 1.79e-009
LLAP_14_29 15 48 1.91e-009
LLAP_15_30 16 49 2.28e-009
KL_1_2 LLAP_1_16 LLAP_2_17 0.3122
KL_1_3 LLAP_1_16 LLAP_3_18 0.113148
KL_1_4 LLAP_1_16 LLAP_4_19 0.0626985
KL_2_3 LLAP_2_17 LLAP_3_18 0.207052
KL_2_4 LLAP_2_17 LLAP_4_19 0.10021
KL_2_5 LLAP_2_17 LLAP_5_20 0.0508199
KL_3_4 LLAP_3_18 LLAP_4_19 0.254314
KL_3_5 LLAP_3_18 LLAP_5_20 0.122646
KL_3_6 LLAP_3_18 LLAP_6_21 0.0594183
KL_4_5 LLAP_4_19 LLAP_5_20 0.25725
KL_4_6 LLAP_4_19 LLAP_6_21 0.115328
KL_5_6 LLAP_5_20 LLAP_6_21 0.247252
KL_5_7 LLAP_5_20 LLAP_7_22 0.0963173
KL_5_8 LLAP_5_20 LLAP_8_23 0.0557342
KL_6_7 LLAP_6_21 LLAP_7_22 0.213059
KL_6_8 LLAP_6_21 LLAP_8_23 0.110235
KL_7_8 LLAP_7_22 LLAP_8_23 0.304107
KL_9_10 LLAP_9_24 LLAP_10_25 0.309416
KL_9_11 LLAP_9_24 LLAP_11_26 0.11293

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```
KL_9_12 LLAP_9_24 LLAP_12_27 0.0649788
KL_10_11 LLAP_10_25 LLAP_11_26 0.21861
KL_10_12 LLAP_10_25 LLAP_12_27 0.113569
KL_11_12 LLAP_11_26 LLAP_12_27 0.264128
KL_11_13 LLAP_11_26 LLAP_13_28 0.113329
KL_11_14 LLAP_11_26 LLAP_14_29 0.0587929
KL_12_13 LLAP_12_27 LLAP_13_28 0.247333
KL_12_14 LLAP_12_27 LLAP_14_29 0.1189
KL_13_14 LLAP_13_28 LLAP_14_29 0.262841
KL_13_15 LLAP_13_28 LLAP_15_30 0.10791
KL_14_15 LLAP_14_29 LLAP_15_30 0.212285
```

```
*LB16 32 33 25P
```

```
*
```

```
* capacitors
```

```
*
```

```
C01 2 34 235F
C02 3 34 194F
C03 4 34 181F
C04 5 34 181F
C05 6 34 181F
C06 7 34 181F
C07 8 34 194F
C08 9 34 235F
C09 10 34 235F
C10 11 34 194F
C11 12 34 182F
C12 13 34 182F
C13 14 34 181F
C14 15 34 181F
C15 16 34 194F
```

```
*
```

```
* mutual capacitors
```

```
*
```

```
C01_02 2 3 127F
C02_03 3 4 47.800F
C03_04 4 5 44.800F
C04_05 5 6 44F
C05_06 6 7 44.700F
C06_07 7 8 47.800F
C07_08 8 9 127F
C09_10 10 11 127F
C10_11 11 12 47.800F
C11_12 12 13 44.700F
C12_13 13 14 44F
C13_14 14 15 44.800F
C14_15 15 16 47.800F
```

```
.ENDS TSSOP16
```

```
*
```

```
.PRINT TRAN V(2001) V(2002)
```

```
*.PROBE
```

```
*
```

```
.END
```