

MAX3262 I/O Model

SPICE I/O Macromodels aid in understanding signal integrity issues in electronic systems. Most of Maxim's High Frequency/Fiber Communication ICs utilize input and output (I/O) circuits with Current Mode Logic (CML), Positive Emitter Coupled Logic (PECL), and Low Voltage Differential Signal (LVDS) formats to transfer data into and out of an IC. These models are based on simplified circuit expressions that may include replacement of active circuit elements with ideal controlled voltage and current sources. As such, simulation with macromodels should be treated as 'typical' performance and not relied upon as final proof-of-design. Use of macromodel descriptions is not a substitute for worst-case design analysis, nor for testing real circuits over temperature, supply, and other operating limits.

The output format is provided as ASCII text netlists suitable for generic SPICE. This format is compatible with most versions of SPICE such as PSPICE and HSPICE. Additional information is found in HFAN 6.1 *Input/Output Models for Maxim Fiber Components*.

To extract the circuit netlists using the Adobe Acrobat Reader follow these instructions. Select the "Text Select Tool" by clicking the left mouse button on this icon of the menu bar (a capital T with a small dashed box to the lower right). Highlight the desired netlist text with the cursor. Use the copy command from the edit menu to capture the selected lines. Then paste the selected lines into a text file editor and save the file with an extension compatible with the simulator.

Revision A1, July 23, 2004

I/O Models for the MAX3262

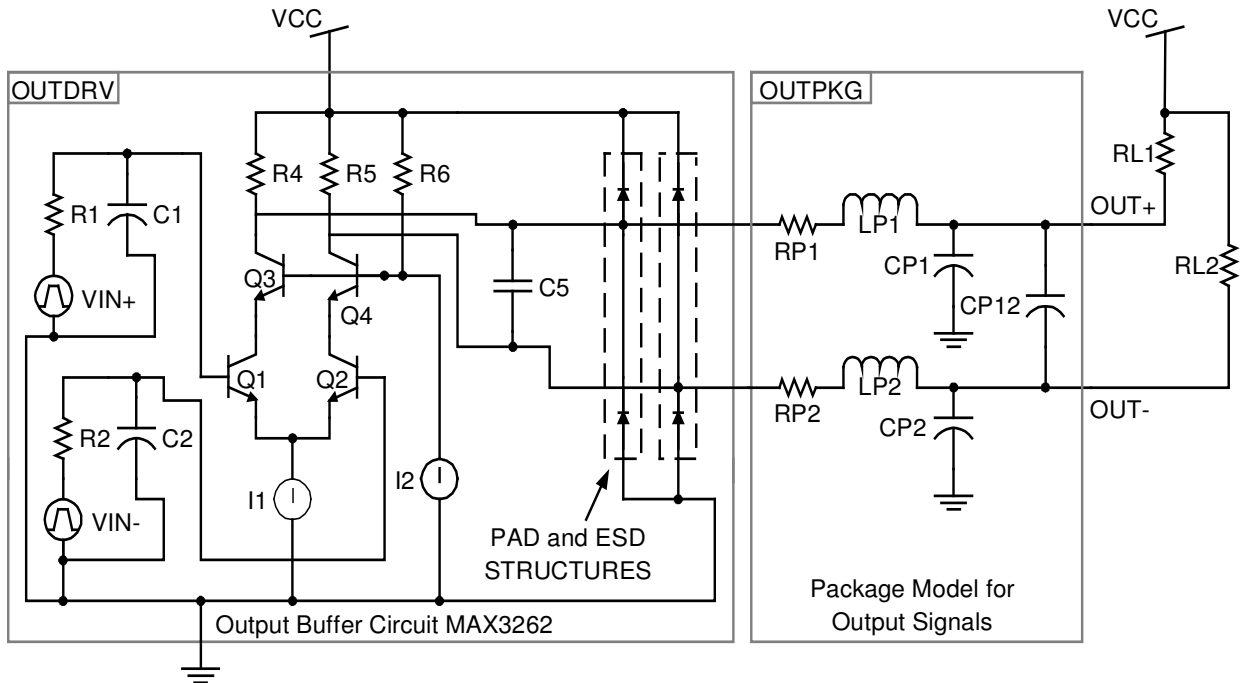


Figure 1. Output model for the MAX3262.

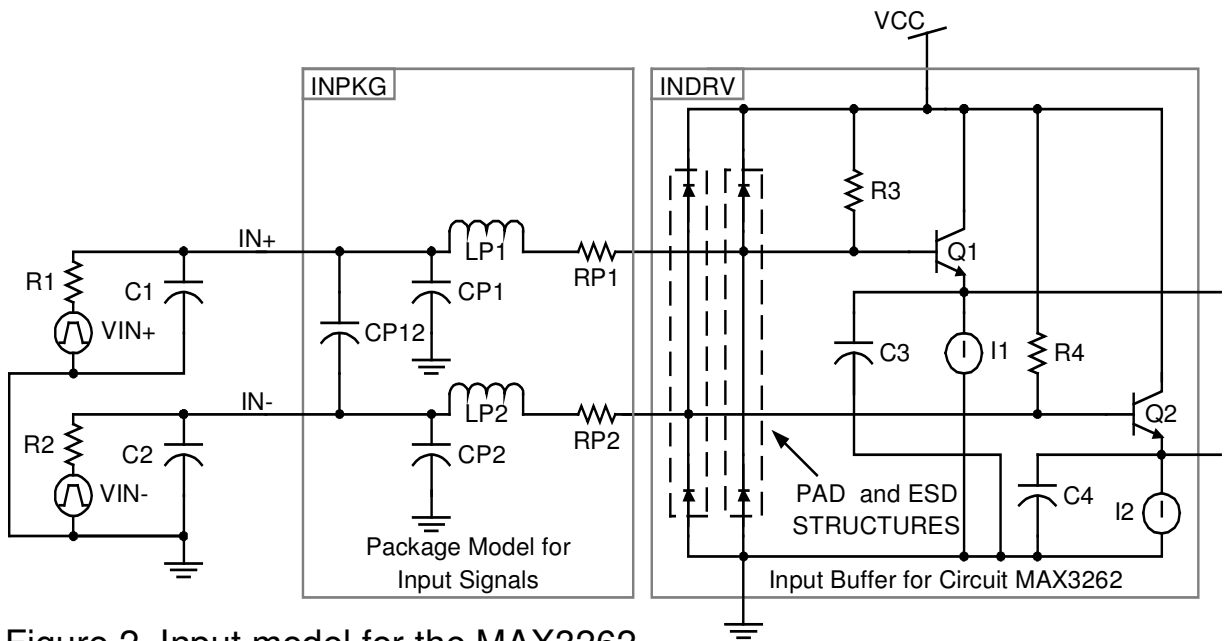


Figure 2. Input model for the MAX3262.

Notes:

The schematics on the previous page represent the output and input stage of the Maxim MAX3262 High Speed Limiting Amplifier. The output circuit shown is for the signal outputs (OUT+, OUT-) and the input circuit is shown with the signal inputs (IN+, IN-). However the models are given in generic SPICE, which only accepts node names as numbers. As discussed in the application note the output signals are described as (2001, 2002) and the input signals are described as (2101, 2102). These models are only valid at 25°C. The bias currents for the input and output circuitry are modeled by ideal current sources. This model is not compensated for variations in VCC, so VCC equal to 5V should be used. The package values have not been calculated and were taken from another model. Pad and ESD structures are implemented in this model.

The Output Stage: The output stage of the MAX3262 is shown as the sub-circuits “OUTDRV” and “OUTPKG”.

The DRV Driver Sub-circuit: The driver sub-circuit is a simplified version of the output stage used by the MAX3262 Limiting Amplifier. The output load is configured with 50 ohm resistors tied to VCC minus 2V. The output is currently configured to be at 600mV peak to peak. The waveform is a pulse whose period is 2ns and has rise and fall times around 250ps. The offset voltage is set at 3.7V. The netlist is given in SPICE 2G6 format in Appendix A

The Input Stage: The input structure of the MAX3262 connects to a differential pair. The input stage has sub-circuits “INDRV” and “INPKG”.

The INDRV Driver Sub-circuit: The input structure of the MAX3262 is connected to an equivalent resistive, capacitive and inductive network of the input package. The input package connects to a emitter follower configuration. The driving voltage source should be set to 0V differential at t=0. This ensures that the two AC coupling capacitors are not charged to different voltages initially (this is the way the circuit operates in steady-state operation). This was achieved by using a piecewise linear source as the driver. See Appendix B for the input netlist.

Text File Format: This model is shipped in “pdf” format. Models and netlists can be copied to text format in the Acrobat Reader by holding the left mouse button on the “Text Select Tool.” Then the user can “select” what netlist and/or subcircuit with the mouse. Then use the copy command from the “edit” menu to capture the selected lines. These lines can then be “pasted” into the user’s text file.

Appendix A: Output Netlist

* 3262 Output File

.OPT ACCT NOMOD LIMPTS=10000

.TEMP 27

.OP

.TRAN 200P 5n

VCC 101 0 4.7V

* Load Resistance

VL 105 0 3

RL1 2001 105 50

RL2 2002 105 50

XOUTPKG 2001 2002 6 16 OUTPKG

XOUTDRV 6 16 101 OUTDRV

.SUBCKT OUTDRV 6 16 101

VINP 2 0 PULSE (1.1 .8 0.0n 0.3n 0.3n .61n 2n)

VINN 12 0 PULSE (.8 1.1 0.0n 0.3n 0.3n .61n 2n)

R1 3 2 100

R2 13 12 100

C1 3 0 2p

C2 13 0 2p

R3 101 6 50

R4 101 16 50

R5 101 7 500

C3 5 0 .1p

C4 15 0 .1p

C5 6 16 .9p

XQ1 5 3 4 0 N402V038_5

XQ2 15 13 4 0 N402V038_5

XQ3 6 7 5 0 N402V066_2

XQ4 16 7 15 0 N402V066_2

I1 4 0 11.87m

I2 7 0 4m

*Pad and ESD Structures

XP1 6 0 PAD4SQ3P7
XP2 16 0 PAD4SQ3P7
XD1 6 101 0 DE0900
XD2 0 6 0 DE0900
XD3 16 101 0 DE0900
XD4 0 16 0 DE0900

.ENDS OUTDRV

.SUBCKT OUTPKG 2001 2002 6 16

RP1 6 7 152M
RP2 16 17 152M
LP1 7 2001 .342N
LP2 17 2002 .342N
CP1 2001 0 178F
CP2 2002 0 178F
CP12 2001 2002 1F

.ENDS OUTPKG

* Transistor Model

.SUBCKT N402V038_5 1 2 3 21

CP1SUB 2 201 25.003F

RP1SUB 20 201 100K

CTRENCH 1 202 60.952F

RFIELDDEPI 202 21 157.563

RREVERT 202 20 1G

CBL 10 20 23.651F

RSUB 20 21 39.497K

CWAFER 20 21 13.338F

CP1EPI 10 12 33.381F

CP1P2 12 3 27.104F

RBX 2 12 4.886 TC=2.052M

RCX 1 10 2.796 TC=2.559M,1.251U

RCI 10 11 699.064M TC=2.559M,1.251U

REX 13 3 1.096

QN 11 12 13 11 TX 5

.MODEL TX NPN(IS=1.606E-017 XTI=3 EG=1.120 BF=380 BR=12 XTB=0 VAF=66

+ VAR=2.500 NF=1.018 NR=1.020 NE=2 NC=1.560 IKF=35.327M IKR=1.004M

+ ISE=8.029E-018 ISC=3.613E-030 RB=6.108 RBM=4.581 IRB=3.613M

+ CJE=37.651F MJE=463M VJE=1.100 FC=990M CJC=19.219F MJC=350M VJC=1

```
+ TF=1.320P TR=5N XTF=2 VTF=1.200 ITF=130.468M PTF=5 KF=10.158N
+ AF=2.150 )
.ENDS N402V038_5
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*****
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```
* Transistor Model
.SUBCKT N402V066_2 1 2 3 21
CP1SUB 2 201 10.001F
RP1SUB 20 201 100K
CTRENCH 1 202 27.253F
RFIELDDEPI 202 21 352.444
RREVERT 202 20 1G
CBL 10 20 14.028F
RSUB 20 21 79.752K
CWAFAER 20 21 6.606F
CP1EPI 10 12 19.271F
CP1P2 12 3 17.035F
RBX 2 12 10.184 TC=1.681M
RCX 1 10 4.485 TC=2.493M,1.163U
RCI 10 11 1.121 TC=2.493M,1.163U
REX 13 3 1.588
QN 11 12 13 11 TX 2
.MODEL TX NPN( IS=2.771E-017 XTI=3 EG=1.120 BF=380 BR=12 XTB=0 VAF=66
+ VAR=2.500 NF=1.018 NR=1.020 NE=2 NC=1.560 IKF=60.952M IKR=1.732M
+ ISE=1.385E-017 ISC=6.234E-030 RB=5.092 RBM=3.819 IRB=6.234M
+ CJE=64.826F MJE=463M VJE=1.100 FC=990M CJC=31.450F MJC=350M VJC=1
+ TF=1.320P TR=5N XTF=2 VTF=1.200 ITF=225.108M PTF=5 KF=16.776N
+ AF=2.150 )
.ENDS N402V066_2
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*****
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*****
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```
* ESD Diode Model
.SUBCKT DE0900 1 2 21
CTRENCH 2 202 58.872F
RFIELDDEPI 202 21 163.328
RREVERT 202 0 1G
CBL 4 5 78.946F
RSUB 5 21 26.725K
CWAFAER 5 21 19.712F
CP1EPI 1 4 76.086F
DD 1 4 DCB
RS 4 2 5.368 TC=4.277M,4.217U
.MODEL DCB D( IS=7.920E-018 N=1.050 CJO=216F VJ=800M M=500M )
.ENDS DE0900
```

* Pad Model

.SUBCKT PAD4SQ3P7 1 3

CPAD 1 10 67.534F

REPI 10 20 378.507 TC=4.800M,5U

CTRENCH 21 20 22.531F

CBL 21 20 1.413P

RX 20 21 1G

RS 3 21 5.416K

CWAFER 21 3 2.587F

.ENDS PAD4SQ3P7

.probe

.END

Appendix B: Input Netlist

* 3262 Input File

.OPT ACCT NOMOD LIMPTS=10000

.TEMP 27

.OP

.TRAN 2PS 3NS

* Voltage Source

VCC 101 0 DC 5V

* Add Input Here. Node 2101 is IN+, Node 2102 is IN-

* Example:

VINP 50 0 PULSE (2.3 1.5 .2n .1n .1n .9n 2n)

VINN 60 0 PULSE (1.5 2.3 .2n .1n .1n .9n 2n)

R1 2101 50 50

R2 2102 60 50

C1 2101 0 .5p

C2 2102 0 .5p

XINPKG 2101 2102 3 13 INPKG

XINDRV 3 13 101 INDRV

.SUBCKT INPKG 2101 2102 3 13

RP1 2 3 152M

RP2 12 13 152M

LP1 2101 2 .342N

LP2 2102 12 .342N

CP1 2101 0 178F

CP2 2102 0 178F

CP12 2101 2102 1F

.ENDS INPKG

.SUBCKT INDRV 3 13 101

R3 101 3 50

R4 101 13 50

C3 4 0 400f
C4 14 0 400f

XQ1 101 3 4 0 N102M066_2
XQ2 101 13 14 0 N102M066_2

I1 4 0 3.6m
I2 14 0 3.6m

* ESD and Pad Structures

XD1 3 101 0 DE0900
XD2 0 3 0 DE0900
XD3 13 101 0 DE0900
XD4 0 13 0 DE0900
XP1 3 0 PAD4SQ3P7
XP2 13 0 PAD4SQ3P7

.ENDS INDRV

* Transistor Model

.SUBCKT N102M066_2 1 2 3 21

CP1SUB 2 201 3.128F

RP1SUB 20 201 100K

CTRENCH 1 202 15.762F

RFIELDDEPI 202 21 608.765

RREVERT 202 20 1G

CBL 10 20 3.956F

RSUB 20 21 169.305K

CWAFER 20 21 3.112F

CP1EPI 10 12 3.835F

CP1P2 12 3 4.423F

RBX 2 12 35.936 TC=1.934M

RCX 1 10 10.159 TC=2.640M,410.600N

RCI 10 11 2.540 TC=2.640M,410.600N

REX 13 3 6.352

QN 11 12 13 11 TX 2

.MODEL TX NPN(IS=6.926E-018 XTI=3 EG=1.120 BF=380 BR=12 XTB=0 VAF=66

+ VAR=2.500 NF=1.018 NR=1.020 NE=2 NC=1.560 IKF=15.238M IKR=432.900U

+ ISE=3.463E-018 ISC=1.558E-030 RB=17.968 RBM=13.476 IRB=1.558M

+ CJE=16.207F MJE=463M VJE=1.100 FC=990M CJC=7.862F MJC=350M VJC=1

+ TF=1.320P TR=5N XTF=2 VTF=1.200 ITF=56.277M PTF=5 KF=82.614N

+ AF=2.150)

.ENDS N102M066_2

* ESD Diode Model

.SUBCKT DE0900 1 2 21
CTRENCH 2 202 58.872F
RFIELDDEPI 202 21 163.328
RREVERT 202 0 1G
CBL 4 5 78.946F
RSUB 5 21 26.725K
CWAFFER 5 21 19.712F
CP1EPI 1 4 76.086F
DD 1 4 DCB
RS 4 2 5.368 TC=4.277M,4.217U
.MODEL DCB D(IS=7.920E-018 N=1.050 CJO=216F VJ=800M M=500M)
.ENDS DE0900

* Pad Model

.SUBCKT PAD4SQ3P7 1 3
CPAD 1 10 67.534F
REPI 10 20 378.507 TC=4.800M,5U
CTRENCH 21 20 22.531F
CBL 21 20 1.413P
RX 20 21 1G
RS 3 21 5.416K
CWAFFER 21 3 2.587F
.ENDS PAD4SQ3P7

.probe
.END