

RELIABILITY REPORT
FOR
MAX3643ETG+
PLASTIC ENCAPSULATED DEVICES

April 16, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
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Conclusion

The MAX3643ETG+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX3643 burst-mode laser driver provides bias and modulation current drive for PON burst-mode ONT applications. It is specifically designed for use with a low-cost external controller for the APC (and if desired, AMC) loop. A high-speed differential burst-enable input enables the driver to switch the laser from a dark (output off) condition to full on condition in less than 2ns. When BEN is inactive, typical modulation and bias currents are 5 μ A each. Laser modulation current can be set from 10mA to 85mA and bias current can be set from 1mA to 70mA using the MODSET and BIASSET inputs. A sample-and-hold circuit is provided to capture the monitor diode output during short PON bursts, if needed, and the BEN high-speed signal is mirrored on an LVCMOS output to be used by the controller operating the APC/AMC loop. The MAX3643 burst-mode laser driver is packaged in a 4mm x 4mm, 24-pin thin QFN package. It operates from -40°C to +85°C.

II. Manufacturing Information

A. Description/Function:	155Mbps to 2.5Gbps Burst-Mode Laser Driver
B. Process:	G4
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	ASAT China, UTL Thailand
F. Date of Initial Production:	October 22, 2005

III. Packaging Information

A. Package Type:	24-pin TQFN 4x4
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2010
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	48°C/W
K. Single Layer Theta Jc:	2.7°C/W
L. Multi Layer Theta Ja:	36°C/W
M. Multi Layer Theta Jc:	2.7°C/W

IV. Die Information

A. Dimensions:	89 X 58 mils
B. Passivation:	Si ₃ N ₄
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn) Metal 1, 2 & 3 5.6 microns (as drawn) Metal 4
F. Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1, 2 & 3, 4.2 microns (as drawn) Metal 4
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.4 \times 10^{-9}$$

$$\lambda = 22.4 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at <http://www.maxim-ic.com/>. Current monitor data for the G4 Process results in a FIT Rate of 0.2 @ 25C and 3.6 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The HT56 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500 V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX3643ETG+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2) 85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2) Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data