

RELIABILITY REPORT
FOR
MAX5922xEUI
PLASTIC ENCAPSULATED DEVICES

June 21, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX5922 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX5922A/B/C is a single-port network power controller with an integrated power MOSFET, operating from a +32V to +60V supply rail. The device is specifically designed for power-sourcing equipment (PSE) in power-over-LAN applications and is fully compliant to the IEEE 802.3af standard. The MAX5922 provides power devices (PD) discovery, classification, current limit, and other necessary functions for an IEEE 802.3af compliant PSE.

The MAX5922 is suitable for PSE function in both switch/router systems where the power is delivered to the load through the signal pairs, and in midspan systems where the power is delivered to the load through the spare pairs. In midspan mode, a detection collision avoidance circuit (MAX5922A/C only) provides the necessary back-off timing to prevent fault detections that happen when two different PSEs try to detect and power the same PD. The MAX5922B/C have a detection disable input that can be connected high to disable the detection/classification functions or connected low to enable them.

The MAX5922 features a programmable undervoltage lockout (UVLO) that keeps the device in shutdown until the input voltage exceeds a certain threshold, set to 38V (MAX5922A) or 28V (MAX5922B/C) internally. After successfully discovering and classifying a PD, the MAX5922 enters startup mode. During startup, the MAX5922 limits the output voltage and current slew rate to minimize EMI (electromagnetic interference). The MAX5922 has an integrated 0.45 Ω N-channel power MOSFET that provides efficient operation and simplified system design. The MAX5922 monitors and provides current-limit protection to the load at all times. The current limit is programmable using an external current-sensing resistor. The MAX5922 features current-limit foldback and duty-cycle limit to ensure robust operation during load-fault and short-circuit conditions. Fault management allows the part to either latch-off or autorestart after a fault.

The MAX5922 provides POK, ZC-bar, and FAULT-bar status signals to indicate output power is good, zero-current fault, and other faults (overcurrent, overtemperature), respectively. The MAX5922 is available in a 28-pin TSSOP package and is rated over the extended -40°C to +85°C temperature range.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
(All voltages with respect to AGND_S, unless otherwise noted.)	
IN	-0.3V to +76V
UVLO	-0.3V to +6V
VDIG to DGND	-0.3V to +6V
OUT	-0.3V to (VDRAIN + 0.3V)
DRAIN	-0.3V to (VIN + 0.3V)
RDT	-0.3V to +12V
RCL to IN	-10V to +0.3V
EN, DET_DIS, DCA, CLASS, ZC_EN, and LATCH to DGND	-0.3V to +6V
POK, ZC, CL0, CL1, CL2, and FAULT to DGND	-0.3V to +6V
DGND	-5V to +5V
Maximum Current into Drain	0.8A
Maximum Current into POK, ZC, CL0, CL1, CL2, FAULT	20mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70C)	
28-PIN TSSOP	1026mW
Derates above +70°C	
28-PIN TSSOP	12.8mW/°C

II. Manufacturing Information

A. Description/Function:	+48V, Single-Port Network Power Switch For Power-Over-LAN
B. Process:	BCD80
C. Number of Device Transistors:	8687
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia or Philippines
F. Date of Initial Production:	March, 2003

III. Packaging Information

A. Package Type:	28-Pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-0448
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1

IV. Die Information

A. Dimensions:	108 X 175 mils
B. Passivation:	$\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

↑
Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 24.13 \times 10^{-9}$$

$$\lambda = 24.13 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6031) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The NP38 die type has been found to have all pins able to withstand a transient pulse of $\pm 400\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX5922xEUI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		45	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TSSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

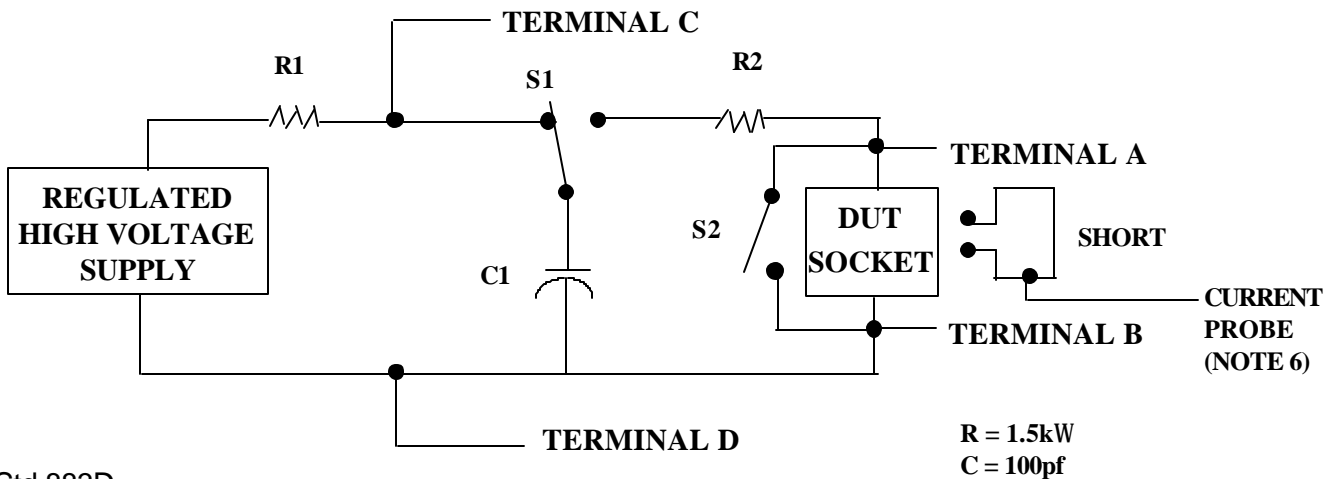
2/ No connects are not to be tested.

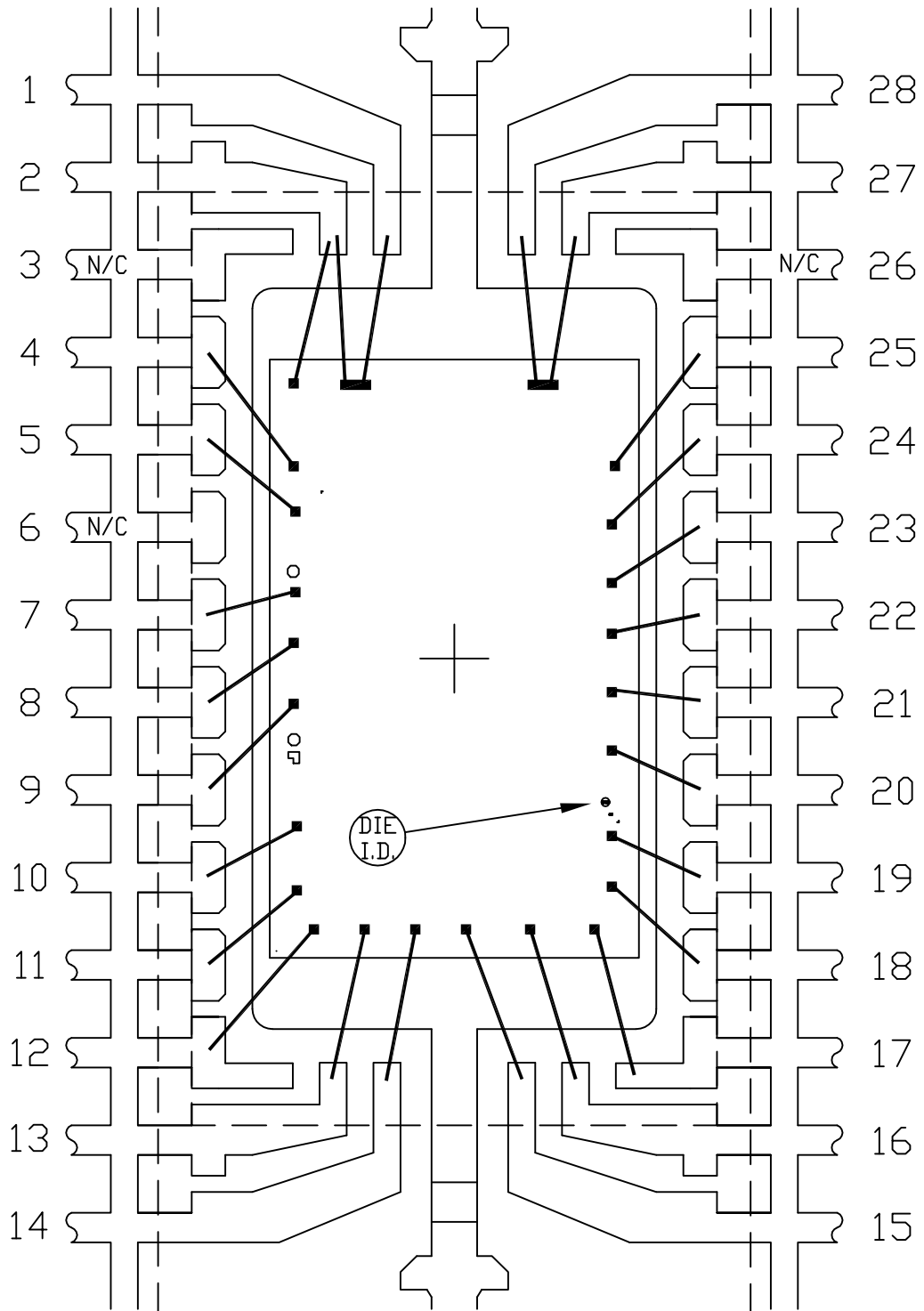
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE: U28-2		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 118x217	PKG. DESIGN			BOND DIAGRAM #: 05-9000-0448	REV: A

