



March 1996

RR-B1A

## ***High-Frequency Bipolar Products Reliability Report***

*This report presents the product reliability data for Maxim's High-Frequency Bipolar analog and digital products. This data was collected from extensive reliability stress tests performed between June 1, 1994 and July 1, 1995. It is separated into four major fabrication processes: 1) SHPi, 9.3GHz two-layer bipolar, 2) GST-1, 12GHz three-layer bipolar, 3) GST-2, 27GHz three-layer bipolar, and 4) CPi, 9.3GHz two-layer with complimentary vertical PNP devices to 5.5GHz.*

*During this testing period, over 1.7 million device operating hours were accumulated for products at an operating junction temperature of +150°C to +165°C. The data in this report is typical of Maxim's production products. As you will see, Maxim's high-frequency bipolar products demonstrate the same high level of reliability you have become accustomed to with our other products and processes.*



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### Fabrication

Maxim is currently running four major high-frequency bipolar processes:

- SHPi ( $f_T = 9.3\text{GHz}$ , two layer)
- GST-1 ( $f_T = 12\text{GHz}$ , three layer)
- GST-2 ( $f_T = 27\text{GHz}$ , three layer)
- CPI ( $f_T = 9.3\text{GHz}$  NPN,  $5.5\text{GHz}$  PNP)

#### SHPi

SHPi is a recessed-oxide-isolated, high-speed, NPN bipolar process designed for superior performance and flexibility (**Figure 1**). It features high-performance vertical NPN transistors ( $f_T = 9.3\text{GHz}$  at  $V_{CE} = 4\text{V}$ ,  $f_{MAX} = 12\text{GHz}$  at  $V_{CE} = 4\text{V}$ ). Minimum NPN transistor area is  $8\mu\text{m} \times 20\mu\text{m}$ . The process features two layers of gold interconnect on  $4\mu\text{m}$  pitch.

#### GST-1

GST-1 (Giga-Speed Si-Bipolar Technology) is a high-speed, self-aligned double-polysilicon process (**Figure 2**). Originating from the research labs of Maxim, GST-1 was designed for building high-density, high-performance circuits. The process employs many techniques, such as Reactive Ion Etching (RIE) and trench isolation, to provide a silicon bipolar platform for high-performance circuit applications to  $12\text{GHz}$ .

#### GST-2

Like GST-1, GST-2 is a high-speed, self-aligned double-polysilicon process (**Figure 3**). The platform was designed for building high-density, high-performance circuits, and employs many of the same processing features as GST-1. GST-2, however, achieves GaAs speed to  $27\text{GHz}$  without GaAs pricing, for up to 200,000 transistors per die.

#### CPI

Like SHPi, CPI is a recessed-oxide-isolated, high-speed, complementary bipolar process designed for superior performance and flexibility (**Figure 1**). Unique to CPI is an optional dual-gate P-channel JFET with one extra mask. However, the feature which most differentiates this process from SHPi is the availability of complimentary vertical PNP transistors with  $f_T = 5.5\text{GHz}$  at  $V_{CE} = 4\text{V}$ .

### Reliability Methodology

Maxim's approach to reliability testing is conservative. Each of the high-frequency bipolar processes is qualified using industry-standard tests and methods as shown in **Table 1**.

The goal for each process is an inherent infant mortality failure rate approaching 300ppm or less. **Table 3** displays the infant mortality data and evaluations accomplished on each of the high-frequency bipolar processes in our Beaverton fabrication facility, as of the date of this publication. Each failure category is prioritized by its relative frequency, to identify which failure mode should be addressed first, second, and so on. This data demonstrates Maxim's goal to provide our customers with the lowest overall cost solution through superior quality products.

Maxim's SHPi, GST-1, GST-2, and CPI high-frequency bipolar processes clearly meet or exceed the performance and reliability expectations of the semiconductor industry.

**TABLE 1: MAXIM PROCESS RELIABILITY TESTS**

TEST NAME	CONDITIONS	SAMPLING PLAN (ACC/SS)
Life Test	+150°C (Tj)/1000 hrs	1/77 or 0/45
85/85	+85°C, 85% RH, 1000 hrs cycled bias	1/77 or 0/45
Pressure Pot	+121°C, 100% RH, 15 PSIG, 168 hrs	0/45*
Temperature Cycling	-55°C to +125°C, air to air, 1000 cycles	1/77 or 0/45
High-Temperature Storage	+150°C, 1000 hrs	1/77 or 0/45

\* Preferred sample size is 77.

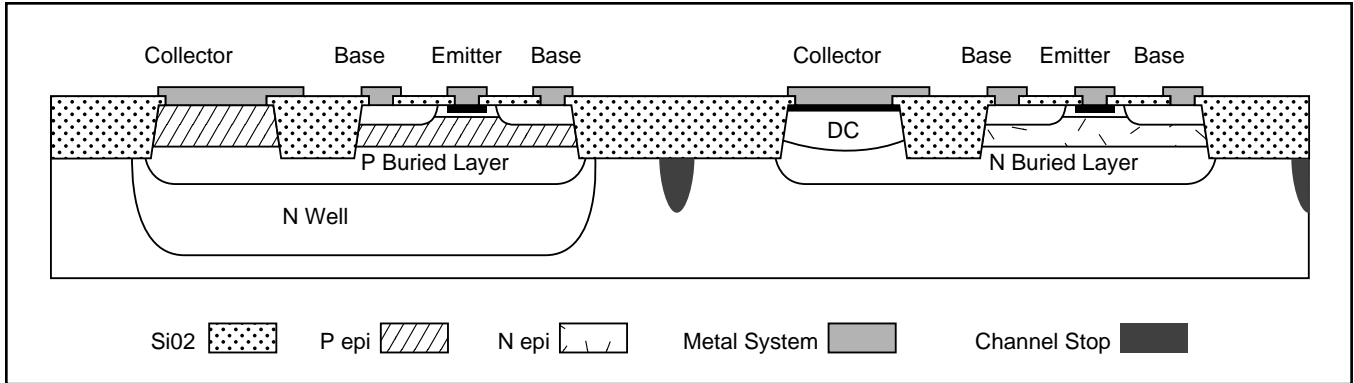


Figure 1: SHPI (NPN Transistor) and CPI (NPN & PNP Transistors) Processes

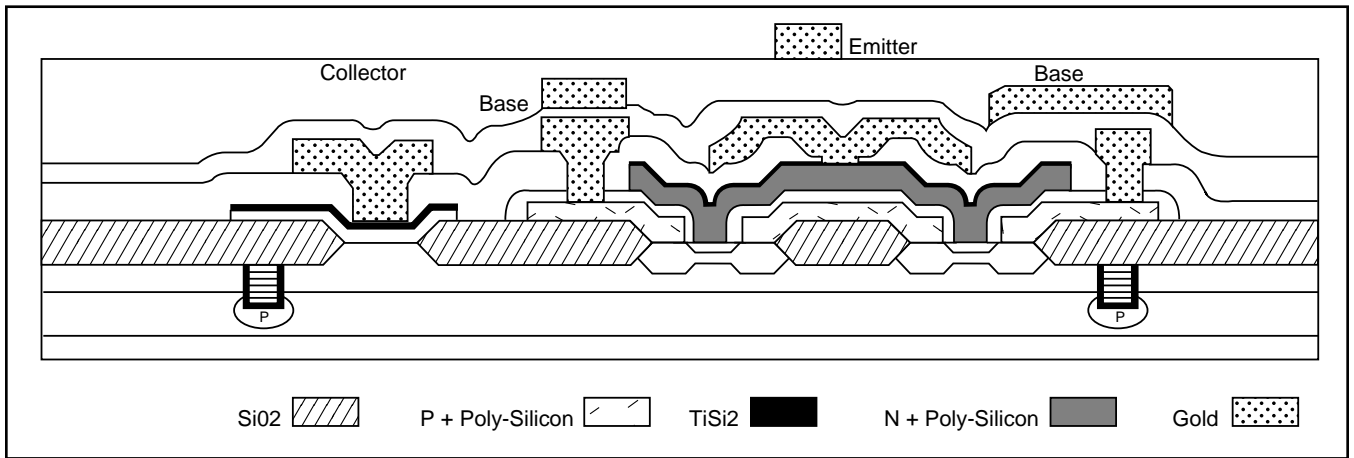


Figure 2: GST-1 Process (NPN Transistor)

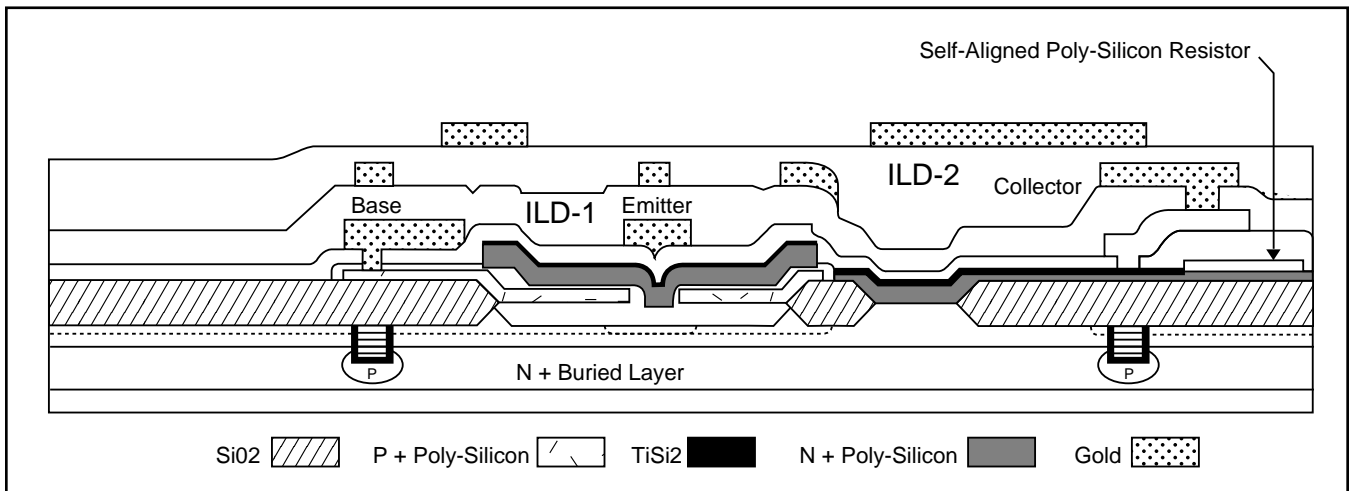


Figure 3: GST-2 Process (NPN Transistor)

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### Reliability Strategy

#### Reliability Program

Maxim has implemented a series of Quality and Reliability programs aimed at building the highest quality, most reliable analog products in the industry. All products, processes, packages, and changes in manufacturing steps must be subjected to Maxim's reliability testing before release to manufacturing for mass production. Our reliability program includes:

- Step 1: Initial Reliability Qualification Program
- Step 2: Ongoing Reliability Monitor Program
- Step 3: In-Depth Failure Analysis and Corrective Action

Tables 4–7 show the results of long-term life testing for each process. Tables 8–11 show similar information for 85/85, Pressure Pot, Temperature Cycling, and High-Temperature Storage testing.

#### Step 1: Initial Reliability Qualification Program

Maxim's product reliability test program meets EIA-JEDEC standards, and most standard OEM reliability test requirements.

Table 1 summarizes the qualification tests that comprise part of Maxim's reliability program. We require that three consecutive manufacturing lots from a new process technology successfully meet these reliability test requirements before releasing products.

#### Step 2: Ongoing Reliability Monitor Program

Maxim identifies specific products from each of the high-frequency bipolar processes on which to perform reliability monitor testing. Each part is subjected to 1000 hours of High-Temperature Operating Life testing, and 168 hours of Pressure Pot testing.

#### Step 3: In-Depth Failure Analysis and Corrective Action

With our technical failure analysis staff, we are capable of handling in-depth analysis of every reliability test failure to the device level. If an alarming reliability failure mechanism or trend is identified, the corrective action will be initiated automatically. This proactive response and feedback ensures that a discrepancy in any device failure mechanism will be corrected before it becomes a major problem.

### Designed-In High Reliability

A disciplined design methodology is an essential ingredient in the manufacturing of a reliable part. No amount of finished product testing can create reliability in a marginal design.

To design-in reliability, Maxim has formulated a set of physical layout rules that yield reliable products, even under worst-case manufacturing tolerances. These rules are rigorously enforced, and every circuit is subjected to computerized Design Rule Checks to ensure compliance.

Maxim pays special attention to Electrostatic Discharge (ESD) protection. Our goal is to design every pin of every product to withstand ESD voltages in excess of 2000 Volts, with the use of a number of available protection schemes. In some cases, the use of protection schemes can limit frequency response, which is unacceptable. In those instances, we take special care to fully identify the ESD hazard level, following the guidelines defined in MIL-STD-883, method 3015. Of course, we use ESD shielding materials to make sure all products are afforded high levels of ESD protection in storage and transit.

### Wafer Inspection

All wafers are fabricated using stable, proven processes with extremely tight control. Each wafer must pass numerous in-process check points, such as oxide thickness, alignment, critical dimensions, defect densities, etc., and must comply with Maxim's demanding electrical and physical specifications.

Finished wafers are inspected optically to detect any physical defects (this is similar to the visual inspection requirements of MIL-STD-883, method 2010).

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### Reliability Testing

#### Life Test

Life testing is performed using static bias conditions that simulate long-term use under application conditions. This test estimates the product's field performance over a long time frame. It establishes, through calculations based on Life Test results, the constant failure-rate level (in FITs), and helps identify any early wearout mechanisms. The device under test is operated at a controlled, elevated ambient temperature to ensure device junctions are



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at +150°C. This test can be used to detect design, manufacturing, silicon contamination, metal integrity, and assembly-related defects.

Table 2 summarizes the data from Life Tests conducted at Maxim's high-frequency bipolar fabrication facility in Beaverton, Oregon. Tables 4–7 display Life Test data for several individual products manufactured on each of those processes.

For information on calculating the failure rates of these products and processes, refer to Appendix 1 of this report.

Test: High-Temperature Operating Life (Life Test)  
 Test Conditions: +150°C operating junction temperature, static bias, 100% duty cycle  
 Failure Criteria: Must meet data sheet specifications  
 Results: See Table 2 and Tables 4–7

### 85/85 (Temperature-Humidity-Bias) Test

The most popular integrated circuit (IC) packaging material is plastic. Plastic packages are not hermetic, therefore moisture and other contaminants can enter the package. Humidity testing can help determine the effects of those contaminants, and may help establish the long-term effects of operating under high levels of humidity.

Maxim tests plastic encapsulated or other non-hermetic packaged products for resistance to long-term effects of moisture using the 85/85 or Temperature-Humidity-Bias (THB) Test. In addition to 85/85 testing, Pressure Pot and HAST (Highly Accelerated Stress Test) can also be used as evaluation tools.

In the 85/85 Test, the device is placed in an atmosphere of +85°C temperature and 85% relative humidity for a period of at least 1000 hours, with bias applied. Most of the high-performance bipolar products tested in our Beaverton facility dissipate enough power so that, if operated with continuous bias, moisture would not penetrate the package. Therefore, we operate the parts at 20% duty cycle (5 minutes on, 25 minutes off) to ensure that moisture enters the package.

Test: 85/85 (THB)  
 Test Conditions: +85°C ambient temperature, 85% relative humidity, static cycled bias (20% duty cycle)  
 Failure Criteria: Must meet data sheet specifications  
 Results: See Table 8

### Pressure Pot Test

The Pressure Pot Test simulates a product's exposure to atmospheric humidity. The object of this evaluation is to cause any corrosive contaminants to react at the die level or bond pads.

Test: Pressure Pot  
 Test Conditions: +121°C ambient temperature, 100% relative humidity, 15 PSIG pressure, unbiased, 168 hours  
 Failure Criteria: Must meet data sheet specifications  
 Results: See Table 9

TABLE 2: LIFE TEST DATA

PROCESS FAMILY	NUMBER OF LOTS TESTED	NUMBER OF FAILURES	TOTAL UNITS TESTED	DEGREES OF FREEDOM	FAILURES IN TIME (FITs)			
					+25°C REF		+75°C REF	
					60%	90%	60%	90%
SHPI	17	0	824	2	0.11	0.28	9.8	24.7
GST-1	11	0	579	2	0.16	0.39	13.9	35.1
GST-2	3	0	231	2	0.39	1.00	34.95	88.06
CPI	3	0	138	2	0.67	1.68	58.5	147.4
Total	34	0	1772	2	0.052	0.131	4.56	11.48

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#### HAST Test

HAST (Highly Accelerated Steam and Temperature, sometimes referred to as Highly Accelerated Stress Test) is replacing 85/85 testing in many instances. Experiments conducted throughout the industry have shown the effects of HAST closely duplicate the effects of 85/85 testing, but in one-tenth the time. Thus, a 1000 hour 85/85 test could be completed in 100 hours through HAST testing. This is an extremely useful test to use for corrective-action verification and/or design-change verification.

Test: HAST  
Test Conditions: +120°C ambient temperature, 85% relative humidity, 9 PSIG pressure, biased, 100 hours minimum  
Failure Criteria: Must meet data sheet specifications

#### Temperature Cycling Test

The Temperature Cycling Test measures a component's response to temperature changes and construction quality. The test cycles parts through a predetermined temperature range (MIL-STD-883, method 1010, class B: -55°C to +125°C, class C: -65°C to +150°C). Fabrication and assembly problems can both be discovered using this test, but it typically identifies any potential quality problems.

Test: Temperature Cycling  
Test Conditions: -55°C air, +125°C air, transition time less than 60 seconds, 15 minute dwell, 1000 cycles  
Failure Criteria: Must meet data sheet specifications  
Results: See Table 10

#### High-Temperature Storage Test

The High-Temperature Storage Test evaluates changes in a product's performance following long-term storage at elevated temperatures. This test is only useful for failure mechanisms which are accelerated by temperature alone.

Test: High-Temperature Storage  
Test Conditions: +150°C ambient temperature, unbiased, 1000 hours  
Failure Criteria: Must meet data sheet specifications  
Results: See Table 1

#### Statistical Process Control

Reliability testing offers little value if the manufacturing process varies widely. A standard assumption, which is often false, is that test samples pulled from production will be representative of the total population. The significance of sample variation can be reduced by increasing the sample size, but unless a process is "in control", variations will negatively affect quality and reliability. Under such conditions, reliability testing may disclose higher than desired failure rates, or widely differing test results.

Maxim monitors the stability of critical process parameters through the use of computerized Statistical Process Control (SPC). This provides our engineers with immediate feedback on process trends and shifts. Using this information, production processes can be maintained to tight tolerances, allowing us to provide the highest possible quality on a continuous basis.

In addition to SPC (for controlling process variation), Maxim uses Design of Experiments methodology to optimize process targeting and increase the "robustness" of each process.

#### Infant Mortality Evaluation

Maxim evaluates the infant mortality of all processes and product families immediately after they achieve qualified status. Through infant mortality analysis, we can identify the common defects for each process or product family. Our goal is to quantify the need for production burn-in. If a 300ppm (parts per million) level can be achieved, the product or process can be manufactured without production burn-in while still ensuring a low infant mortality rate. Refer to Table 3 for the current data on Maxim's low product infant mortality rate.



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**TABLE 3: INFANT MORTALITY EVALUATION RESULTS**

PRODUCT	LOT	BI TEMP	SS	FAIL	PPM	ANALYSIS
<b>SH3 PROCESS*</b>						
155-0289-02	LE10XXX	145	95	0	0	
	L501XXX	145	762	0	0	
	L502XXX	145	963	0	0	
	M41XXXX	145	1362	0	0	
	L503XXX	145	1310	0	0	
	L504XXX	145	1694	0	0	
155-0290-02	BE100XX	145	104	0	0	1 metal defect, 1 marginal trim
	M41XXXX	145	671	0	0	
	L501XXX	145	566	2	3525	
	L502XXX	145	719	0	0	
	L503XXX	145	767	0	0	
	L504XXX	145	220	0	0	
155-0371-02 (203-2653-01 die)	M502XXX	150	92	0	0	
	M503XXX	150	495	0	0	
	M504XXX	150	1054	0	0	
	M505XXX	150	481	0	0	
	M506XXX	150	324	0	0	
	M507XXX	150	1126	0	0	
	M508XXX	150	569	0	0	
	M509XXX	150	194	0	0	
<b>Subtotal</b>	<b>20 Lots</b>		<b>13,568</b>	<b>2</b>	<b>147</b>	
<b>GST-1 PROCESS</b>						
155-0371-02 (203-2726-01 die)	M502XXX	150	92	0		1 VOS shift 1 M1-M1 short, 1 CE leak.  Mechanical damage on die surface.  Mechanical damage on die surface.
	M503XXX	150	495	0	2850	
	M504XXX	150	1054	3		
	M505XXX	150	481	1	2080	
	M506XXX	150	324	1	3085	
	M507XXX	150	1126	0	0	
	M508XXX	150	569	0	0	
	M509XXX	150	194	0	0	
<b>Subtotal</b>	<b>8 Lots</b>		<b>4335</b>	<b>5</b>	<b>1155</b>	
<b>SHHV PROCESS*</b>						
806-0004-22	M501XXX	150	1035	0	0	
	M503XXX	150	298	0	0	
	M506XXX	150	348	0	0	
	Q510XXX	150	67	0	0	
155-00241-02	L504XXX	150	578	0	0	
	L508XXX	150	666	0	0	
	L510XXX	150	418	0	0	
<b>Subtotal</b>	<b>7 Lots</b>		<b>3410</b>	<b>0</b>	<b>0</b>	

\* SH3 and SHHV processes are being phased out through use of GST-1 and GST-2 processes.

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**TABLE 3: INFANT MORTALITY EVALUATION RESULTS (continued)**

PRODUCT	LOT	BI TEMP	SS	FAIL	PPM	ANALYSIS
<b>SHPi PROCESS</b>						
806-0089-23	M502XXX	150	885	0	0	
	M503XXX	150	2669	0	0	
	M506XXX	150	1571	0	0	
	Q507056	150	384	0	0	
806-0015-02	M501XXX	160	200	1	5000	Laser wafer-trimmed resistor shift**
	M503XXX	160	107	0	0	
	M504XXX	160	275	2	7275	Laser wafer-trimmed resistor shift**
	M505XXX	160	100	0	0	
	Q507XXX	160	200	0	0	
	M509XXX	160	390	1	2565	Laser wafer-trimmed resistor shift**
	M503XXX	160	244	0	0	
	M504XXX	160	502	1	1995	Laser wafer-trimmed resistor shift**
	M505XXX	160	210	0	0	
	M506XXX	160	792	0	0	
	M507XXX	160	1170	2	1710	Laser wafer-trimmed resistor shift**
	M508XXX	160	270	0	0	
	X509XXX	160	399	0	0	
	Q510XXX	160	107	0	0	
Subtotal	18 Lots		10,475	7	688	
COMBINED TOTALS			31,788	9	283	

\*\* Burn-in implemented to screen for resistor shift on trimmed precision resistors (24-hour burn-in).

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### Field Failure Analysis

In addition to careful analysis of infant mortality failures, Maxim emphasizes analysis of returns from customers, to determine failure modes that can not be observed except through extensive long-term exposure in applications.

The information obtained from this analysis is also a useful tool in prioritizing quality improvement throughout the facility, from wafer fabrication through final test and shipping.

A recent summary of failure sources for customer returns is shown in the graph of Figure 4.

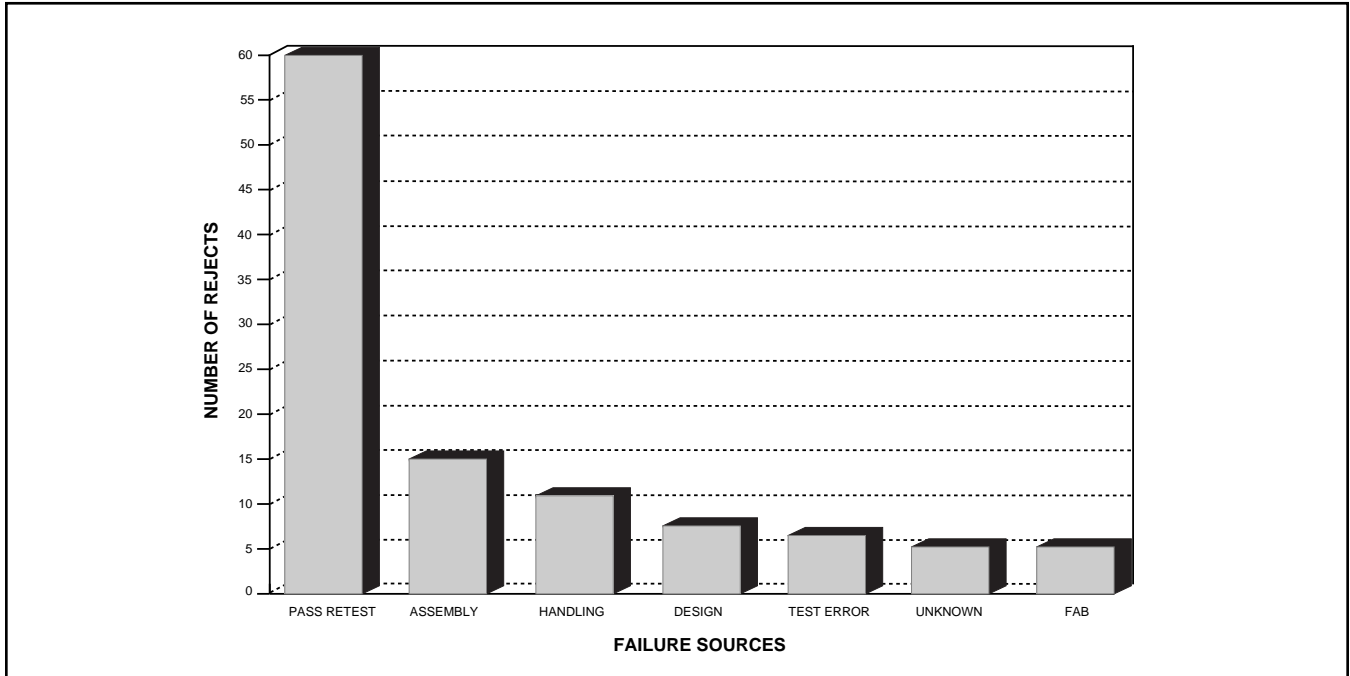


Figure 4: Failure Analysis (Customer Returns)

### Reliability Test Results

TABLE 4: LIFE TEST DATA—SHPI PROCESS

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES*		
				T1	T2	T3
234-1115-20	9406	80 MQUAD	42	0	0	0
806-0003-20	9430	28 PLCC	40	0	0	0
806-0003-20	9419	28 PLCC	45	0	0	0
806-0089-23	9450	28 CLCC	40	0	0	0
806-0089-23	9502	28 CLCC	40	0	0	0
806-0189-31	NR	28 PLCC	77	0	0	0
806-0189-31	9447	28 PLCC	77	0	0	0
806-0227-40	9444	48 SQFP	38	0	0	0
806-0227-40	9444	48 SQFP	39	0	0	0
806-0227-40	9406	48 SQFP	40	0	0	0
806-0227-40	9433	48 SQFP	40	0	0	0
806-0232-22	9440	44 TEQ	30	0	0	0
806-0232-22	9448	44 TEQ	45	0	0	0
806-0232-22	9451	44 TEQ	45	0	0	0
806-0232-22	9502	44 PQUAD	30	0	0	0
MAX4005	9442	8 SOIC	84	0	0	0
MAX555	9502	68 TEQ	72	0	0	0

TABLE 5: LIFE TEST DATA—GST-1 PROCESS

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES*		
				T1	T2	T3
155-0371-02	9447	84 MLC	45	0	0	0
806-0258-20	9410	32 PLCC	40	0	0	0
MAX2101	9502	100 MQFP	150	0	-	-
MAX2101	9452	100 PQUAD	45	0	0	0
MAX2101	9411	100 MQFP	45	0	0	0
MAX2101	9434	100 MQFP	44	0	0	0
MAX2101	9443	100 MQFP	40	0	0	0
MAX3261	9505	32 TQFP	45	0	0	0
MAX3261	9437	32 TQFP	45	0	0	0
MAX3262	9504	24 SSOP	65	0	-	-
MAX3260	9426	20 PDIP	60	0	0	0

\* T1 = 192 hours, T2 = 500 hours, T3 = 1000 hours.

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**TABLE 6: LIFE TEST DATA—GST-2 PROCESS**

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES*		
				T1	T2	T3
806-0300-20	9440	20 PDIP	77	0	0	0
806-0300-20	9445	20 PDIP	77	0	0	0
806-0300-20	9503	20 PDIP	77	0	0	0

**TABLE 7: LIFE TEST DATA—CPI PROCESS**

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES*		
				T1	T2	T3
234-1504-20	NR	44 PLCC	46	0	0	0
234-1504-20	NR	44 PLCC	46	0	0	0
234-1504-20	NR	44 PLCC	46	0	0	0

**TABLE 8: 85/85 (THB) TEST DATA**

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES			NOTES
				168 Hours	500 Hours	1000 Hours	
155-0371-02	9447	84 MLC	18	0	0	0	
234-1115-20	9406	80 MQUAD	36	0	0	0	
234-1504-20	NR	44 PLCC	22	0	0	0	
234-1504-20	NR	44 PLCC	44	0	0	0	
234-1504-20	NR	44 PLCC	44	1	1	0	Ball bond failure (2)
806-0003-20	9430	28 PLCC	40	0	0	0	
806-0003-20	9410	28 PLCC	45	0	0	1	Ball bond failure
806-0004-22	9081	24 PPDIP	45	0	0	0	
806-0004-22	9437	24 PPDIP	45	0	0	0	
806-0004-22	9426	24 PPDIP	45	0	0	5	Ni corrosion
806-0189-31	9447	28 PLCC	45	0	0	0	
806-0189-31	NR	28 PLCC	45	0	0	0	
MAX2101	9452	100 MQFP	45	0	0	0	
MAX2101	9434	100 MQFP	35	0	0	0	
MAX2101	9411	100 MQFP	45	0	0	0	
MAX2101	9443	100 MQFP	45	0	0	0	
806-0227-40	9406	48 SQFP	25	0	0	0	
806-0227-40	9433	48 SQFP	25	0	0	0	
806-0227-40	9444	48 SQFP	38	0	0	0	
806-0227-40	9444	48 SQFP	39	0	0	0	
806-0258-20	9410	32 PLCC	25	0	0	0	
806-0300-20	9440	20 PDIP	45	0	0	0	
806-0300-20	9445	20 PDIP	75	0	0	0	
806-0300-20	9503	20 PDIP	75	0	0	0	
MAX100	NR	84 MLC	16	0	0	0	
MAX100	NR	84 MLC	29	0	0	0	
MAX3261	9437	32 TQFP	44	0	0	0	
MAX555	9502	68 TEQ	80	0	0	0	

**TABLE 9: PRESSURE POT TEST DATA (+121°C, 15 PSI, 100% RH)**

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES (168 Hours)	NOTES
155-0371-02	9447	84 MLC	15	0	
234-1504-20	NR	44 PLCC	45	0	
234-1504-20	NR	44 PLCC	45	0	
234-1504-20	NR	44 PLCC	45	0	
806-0003-20	9430	28 PLCC	40	0	
806-0003-20	9410	28 PLCC	45	2	Ball bond failure
806-0004-22	9081	24 PPDIP	45	0	
806-0004-22	9437	24 PPDIP	45	0	
806-0004-22	9426	24 PPDIP	45	0	
806-0089-23	9450	28 CLCC	45	0	
806-0089-23	9502	28 CLCC	45	0	
MAX2101	9452	100 MQFP	45	0	
MAX2101	9443	100 MQFP	40	0	
MAX2101	9427	100 MQFP	45	0	
MAX2101	9434	100 MQFP	45	0	

\* T1 = 192 hours, T2 = 500 hours, T3 = 1000 hours.



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TABLE 9: PRESSURE POT TEST DATA (+121°C, 15 PSI, 100% RH) (continued)

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES (168 Hours)	NOTES
806-0227-40	9406	48 SQFP	15	0	
806-0227-40	9433	48 SQFP	25	0	
806-0227-40	9444	48 SQFP	45	0	
806-0232-22	9448	44 TEQ	10	0	
806-0232-22	9451	44 TEQ	30	0	
806-0232-22	9440	44 TEQ	45	0	
806-0232-2X	9502	44 PQUAD	45	0	
806-0258-20	9410	32 PLCC	15	0	
MAX3261	9505	32 TQFP	45	0	
MAX3261	9437	32 TQFP	30	0	
806-0300-20	9440	20 PDIP	45	0	
806-0300-20	9445	20 PDIP	45	0	
806-0300-20	9503	20 PDIP	45	0	
MAX100	NR	84 MLC	15	0	
MAX555	9084	68 TEQ	35	7	LWT shift**
MAX555	9502	68 TEQ	20	0	

\*\* Laser Wafer Trimmed precision resistor shift. Burn-in implemented as screen for product.

TABLE 10: TEMPERATURE CYCLING TEST DATA (-55°C TO +125°C, 1000 CYCLES)

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES		
				200 Cycles	500 Cycles	1000 Cycles
155-0371-02	9447	84 MLC	20	0	0	0
234-1115-20	9406	80 MQUAD	43	0	0	0
234-1504-20	NR	44 PLCC	45	0	0	0
234-1504-20	NR	44 PLCC	45	0	0	0
234-1504-20	NR	44 PLCC	45	0	0	0
806-0003-20	9419	28 PLCC	45	0	0	0
806-0003-20	9430	28 PLCC	45	0	0	0
806-0004-22	9026	24 PPDIP	45	0	0	0
806-0004-22	9437	24 PPDIP	45	0	0	0
806-0004-22	9450	24 PPDIP	45	0	0	0
806-0089-23	9502	28 CLCC	45	0	0	0
806-0089-23	9502	28 CLCC	45	0	0	0
806-0089-23	9450	28 CLCC	45	0	0	0
MAX2101	9452	100 MQFP	45	0	0	0
MAX2101	9434	100 MQFP	41	0	0	0
MAX2101	9427	100 MQFP	45	0	0	0
MAX2101	9443	100 MQFP	40	0	0	0
806-0227-40	9406	48 SQFP	25	0	0	0
806-0227-40	9433	48 SQFP	30	0	0	0
806-0227-40	9444	48 SQFP	45	0	0	0
806-0232-22	9440	44 TEQ	45	0	0	0
806-0232-22	9448	44 TEQ	45	0	0	0
806-0232-22	9451	44 TEQ	45	0	0	0
806-0232-2X	9502	44 PQUAD	45	0	0	0
806-0258-20	9410	32 PLCC	110	0	-	-
806-0300-20	9440	20 PDIP	36	0	0	0
806-0300-20	9445	20 PDIP	45	0	0	0
806-0300-20	9503	20 PDIP	45	0	0	0
MAX3261	9437	32 TQFP	45	0	0	0
MAX3261	9505	32 TQFP	45	0	0	0
MAX555	9502	68 TEQ	45	0	0	0

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**TABLE 11: HIGH-TEMPERATURE STORAGE TEST DATA (+150°C, 1000 HRS)**

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES			NOTES
				168 Hours	500 Hours	1000 Hours	
155-0371-02	9447	84 MLC	15	0	0	0	
234-1115-20	9406	80 MQUAD	45	0	0	0	
234-1504-20	NR	44 PLCC	45	0	0	0	
234-1504-20	NR	44 PLCC	45	0	0	0	
234-1504-20	NR	44 PLCC	45	0	0	0	
806-0003-20	9430	28 PLCC	30	0	0	0	
806-0003-20	9419	28 PLCC	45	0	0	0	
806-0004-22	9081	24 PPDIP	45	0	0	0	
806-0004-22	9437	24 PPDIP	45	0	0	0	
806-0004-22	9426	24 PPDIP	45	0	0	0	
806-0089-23	9450	28 CLCC	30	0	0	0	
806-0089-23	9502	28 CLCC	30	0	0	0	
806-0089-23	9502	28 CLCC	30	0	0	0	
MAX2101	9452	100 MQFP	40	0	0	0	
MAX2101	9443	100 MQFP	30	0	0	0	
MAX2101	9427	100 MQFP	45	0	0	0	
MAX2101	9434	100 MQFP	45	0	0	0	
806-0227-40	9406	48 SQFP	40	0	0	0	
806-0227-40	9433	48 SQFP	25	0	0	0	
806-0227-40	9444	48 SQFP	45	0	0	0	
806-0232-22	9448	44 TEQ	40	0	0	0	
806-0232-22	9451	44 TEQ	30	0	0	0	
806-0232-22	9440	44 TEQ	45	0	0	0	
806-0232-2X	9502	44 PQUAD	38	0	0	0	
MAX3261	9505	32 TQFP	45	0	0	0	
MAX3261	9437	32 TQFP	45	0	0	0	
806-0300-20	9440	20 PDIP	45	0	0	0	
806-0300-20	9445	20 PDIP	45	0	0	0	
806-0300-20	9503	20 PDIP	45	0	0	0	
MAX555	9084	68 TEQ	28	0	8	8	LWT shift**
MAX555	9502	68 TEQ	37	0	0	0	

\*\* Laser Wafer Trimmed precision resistor shift. Burn-in implemented as screen.

### Appendices

#### Appendix 1: Determining Acceleration Factor

##### Definition of Terms

An acceleration factor is a constant used in reliability prediction formulas that expresses the effect of temperature on a device's failure rate over time. Generally, semiconductor devices degrade faster as temperature increases. For that reason, operating devices at elevated temperatures allows long-term testing to be accomplished at an accelerated rate, shortening the overall time needed to verify good reliability failure rates. In simple terms, a statement such as, "The failure rate of these devices operating at +150°C is 369 times greater than the failure rate at +75°C," implies an acceleration factor of 369.

The acceleration factor typically used throughout the semiconductor industry is derived using the Arrhenius equation:

$$\text{Acceleration Factor (AF)} = e^{\frac{E_a}{k} \left( \frac{1}{T_1} - \frac{1}{T_2} \right)}$$

- Where:
- Ea = activation energy (electron volts)
  - k = Boltzmann's constant
  - T1 = derating temperature (Kelvin)
  - T2 = acceleration temperature (Kelvin)

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## How to Use the Arrhenius Equation

The first step in calculating an acceleration factor is to determine the activation energy for the predominant failure mechanism. This can be done quantitatively by observing the mechanism of failure and selecting an activation energy from numerous existing tables. For example, intermetallic growth is defined as an activation energy of 1.0eV, oxide pinholes is 0.7eV, etc.

To qualitatively define the activation energy, one must first derive the value through experimentation. Failure analysis techniques are employed to determine failure mechanisms for devices that have failed as a result of high-temperature stress testing. Once the primary mechanism has been identified, additional Life Tests at various elevated temperatures may be performed, and continue until some percentage of the population fails for that mechanism. From that information, a calculation can be created which defines the activation energy, in electron volts.

Assuming two groups of samples have been run at two different temperatures, the number of failures from both groups is totaled:

Group 1: 9822 failures after 100 hrs operation at +150°C

Group 2: 1 failure after 100 hours operation at +25°C

The acceleration factor for the failure mechanism between the two temperatures is 9822 / 1, or 9822.

The Arrhenius equation can be rewritten as follows:

$$AF = 9822 = e^{\frac{E_a}{k} \left( \frac{1}{T_1} - \frac{1}{T_2} \right)}$$

Where:  $E_a$  = unknown

$k$  =  $8.63 \times 10^{-5} \text{eV} / ^\circ\text{K}$

$T_1$  = +25°C + +273°C (298K)

$T_2$  = +150°C + +273°C (423K)

Solving the equation for the activation energy results in approximately 0.8eV.

Assuming the activation energy found represents the dominant failure mechanism of the device under consideration, it may then be used to determine the acceleration factor between any two temperatures. For example, if the test temperature is +150°C and the application (derating) temperature is +70°C, the calculation for acceleration factor, with 0.8eV activation energy, is 165.

## Appendix 2: Determining Failure Rate

### Definition of Terms

The Mean Time Between Failures (MTBF) is the average time it takes for a failure to occur. For example, assume a company tests 100 units for 1000 hours. The total device-hours accrued would be 100 x 1000, or 100,000 device-hours. Now assume two units were found to be failures. Roughly, it could be said the MTBF would equal:

$$MTBF = \frac{\text{Total device-hours}}{\text{Total no. of failures}} = \frac{100,000}{2} = 50,000$$

The failure rate is equal to the reciprocal of the MTBF, or:

$$\text{Failure Rate} = \frac{1}{MTBF} = \frac{1}{50,000} = 0.00002$$

Multiplying this number by  $1 \times 10^5$  yields the failure rate, in terms of percent per 1000 hours. For our example, the failure rate is 0.2%.

A common reliability term also used to express the failure rate is Failures-in-Time, or FIT. This is the number of failures per one billion device-hours, and is obtained by dividing the failure rate by  $10^{-9}$ . Continuing with the example above, the failure rate in FITs is:

$$0.00002 / 10^{-9} = 20,000$$

The FIT rate is, therefore, the number of units predicted to fail in one billion ( $10^9$ ) device-hours at a specific temperature.

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### Calculating Failure Rates and FITs

The failure rate can be expressed in terms of the following four variables:

- A = number of failures observed
- B = number of hours the test was run
- C = number of samples used
- D = temperature acceleration factor

Assume the following is true:

- A = 2
- B = 1000 hours (HTOL)
- C = 824
- D = temperature acceleration factor

Where:

$$D = e^{\frac{0.8}{8.63 \times 10^{-5}} \times \left( \frac{1}{T_1} - \frac{1}{T_2} \right)}$$

$$= e^{\left[ 9269.98 \times \left( \frac{1}{298} - \frac{1}{423} \right) \right]}$$

$$= 9960$$

Substituting into the equation for failure rate:

$$FR = 1 / MTBF$$

$$= 1 / [(B \times C \times D) / 2]$$

$$= 1 / [(1000 \times 824 \times 9960) / 2]$$

$$= 1 / (8,207,040 / 2)$$

$$= 2.436 \times 10^{-10}$$

Converting to FITs by multiplying by  $10^9$ , the failure rate is 0.2436 FITs.

### Including Statistical Effects in the FIT Calculation

Because a small random sample is being chosen from each lot, the statistical effects are significant enough to mention. With most published failure-rate figures, there is an associated confidence level number. This number expresses the confidence level that the actual failure rate of the lot will be equal to, or lower than, the predicted failure rate.

The failure-rate calculation, including a confidence level, is determined as follows:

$$FR = x^2 / 2DH$$

Where:

- $x^2$  = the Chi square value
- 2DH = 2 times the total device hours
- = 2 x ( B x C x D )

The Chi square value is based on a particular type of statistical distribution. However, all that is required to arrive at this value is knowing the number of failures. In this example there were two failures and, using a Chi square distribution table, a value of 6.21 is found. Thus, with a 60% confidence level, the failure rate for our example is:

$$FR = 6.21 / 2 \times 8.207 \times 10^9$$

$$= 3.7831 \times 10^{-10}$$

$$= 0.378 \text{ FITs}$$